ESD Protection Design Using Copper Interconnects: More Robustness And Less Parasitics

A Phase Two Report
Submitted to SRC Copper Design Contest 1999

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(Final Report)

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ABSTRACT

This report presents a comprehensive investigation on the advantages of using copper interconnects in ESD protection designs. 4KV GGMOS ESD protection structures using Cu interconnects, a 2GHz ring oscillator circuit and a low-power, high-speed Op Amp circuit were designed for comparison study. In Phase I, simulation results show that, while ESD protection devices may inevitably affect circuit operation, the use of Cu interconnects can not only significantly improve the ESD robustness (> +30%) but also substantially reduce the unavoidable negative influences (~ +20%) of the ESD protection devices on the core IC chips protected. In Phase II, the simulation findings were partially confirmed by measurement data. Testing results for individual Cu ESD metal test structures match the simulation reasonably well, which proved that Cu indeed provides superior ESD performance compared with Al. It also confirmed that, using ESD simulation, much less ESD metal coverage is actually needed to assure same ESD protection than that suggested by traditional ESD metal design rules. Alternatively, these findings suggest that substantially less ESD-induced parasitic effects on overall circuit performance may be expected in Cu technology compared with its Al counterpart for adequate ESD protection. This work clearly demonstrates the benefits of using Cu interconnects in high-speed designs to realize both higher ESD robustness and lower ESD-related parasitic effects as compared to the traditional Al interconnects. Unfortunately, the latter argument cannot be confirmed in measurements because our circuits do not function properly due to missing N+ layers.

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OBJECTIVES

1. Using a novel mixed-mode TCAD-ECAD ESD simulation-design methodology, which simulates both silicon devices and metal interconnects simultaneously, to demonstrate that copper interconnects may provide better ESD robustness compared to the traditional aluminum interconnects.

2. To demonstrate that narrower copper metal lines are needed to achieve the same level of ESD performance as compared to aluminum interconnects, therefore, dramatically reduce the ESD-oriented parasitic capacitances, which may cause substantial performance degradation of the circuits protected.

3. To demonstrate that using copper interconnect technology can simultaneously improve ESD robustness and reduce circuit performance deterioration caused by ESD-related parasitic capacitances.

4. To serve as ESD design guidelines in using copper interconnect technology.

INTRODUCTION

On-chip Electrostatic Discharge protection design emerges as a major challenge as IC technologies migrate into the very deep sub-micron (*VDSM*) regime [1], because ESD protection units consume significant amount of Si area. On the other hand, the parasitic effects (both capacitive and resistive) from the ESD structures are becoming an intolerable design issue in high-speed IC designs. These days, designers start to take into consideration the metal interconnect-related time delay in global design planning, however, few designers really pay any attention to the potential negative impacts of ESD protection structures on the core IC chips. In dealing with ESD protection design, one normally only considers such destructive effects from ESD units as latch-up and inadequate protection, etc. Nevertheless, just like the attentions paid to the global interconnect time issues, one must consider the parasitic effects of ESD structures on core IC circuits in high frequency design, *e.g.*, in advanced RF IC design. Especially, as marketing strategy driving ESD specification level higher and higher (aggressive IC vendors are offering > HBM 8KV for mixed-signal chips and HBM 4KV for CMOS logic chips), the size of ESD structures are getting larger that makes ESD parasitic effect even more severe. Designers start to realize that in mixed-signal design, traditional CMOS ESD structures are less attractive because of the size. Research in compact ESD design is becoming very active recently. One major source of parasitic ESD capacitance (C_{ESD}) is the metal line induced capacitance. The reason is that, while many novel ESD structures have been invented, little has been done in terms of optimization of ESD metal lines. Virtually nobody can answer how wide a metal line is needed for a specific ESD protection level. The current rule of thumb in selecting ESD metal line width is ~20um universally (as confirmed by the suggestion from our design sponsor, UMC[2]), or, "better make it wide". The major problem behind this rule is that, there has been no practical ESD simulation method that can be used to predict ESD design forwardly, meaning not just trying to match the ESD design after the silicons -- a backward make-up means. There is currently no existing approach that may simulate both the Si devices and metal lines altogether in ESD design. The problem, therefore, is two folds: On one hand, a fixed ESD metal width may not be adequate for any ESD compliance level (i.e., 20um for 2KV, 4KV, or 10KV?). On the other hand, in most high-speed designs, the nominal 20um ESD metal line may be much more than what is needed, therefore produces too much C_{ESD}. There are two questions a designer should ask in ESD design. First, what minimum ESD metal line is enough with some safety margin? Second, how much negative impact from ESD units will be seen by the core circuits? It is well known that the new copper interconnect technology delivers many benefits in improving IC performance, compared to the traditional aluminum interconnects. It is also reported that copper interconnects improve IC reliability in terms of both electromigration and ESD performance[3]. However, so far, there have been no publications addressing such practical questions concerning IC designers. For example, really how wide a metal should I use in my design? How much ESD parasitic effect does my chip face? What benefits do I get in

ESD design if using the expensive and not-yet-reliable copper interconnect technology? Can copper technology simultaneously improve ESD robustness and circuit performance? The fact that the UMC 0.18μm Cu and Al technologies share the *same* ESD design rules for metal lines[2] (and almost same AC electromigration rules for single pulse), although their DC electromigration rules show significant different between Cu and Al[7,8], further confirms such observation that, in industrial practices, no optimized ESD metal design rules exist currently. Unfortunately, the current rules-of-thumb in ESD design do not hold in high-frequency designs using Cu interconnects. The goal of this contest work is trying to answer the above questions by demonstrating better ESD robustness and reduced ESD side-effect on core circuit performance when using copper interconnect technology. It also serves to provide a practical ESD simulation-design methodology and guidelines dealing with selection of ESD metal line width in designs.

DESIGN STRATEGY

The goal of this design work is to demonstrate that there are, at least, two benefits in using copper interconnect technology compared to using aluminum interconnect: improved ESD robustness level with the same or narrower ESD metal line; and substantial reduction in ESD-induced (C_{ESD}) IC performance degradation. We will leave it with other teams to demonstrate how well copper interconnects can improve circuit performance itself. The following design strategy was developed to achieve this project goal.

***Design to show better Cu-ESD robustness*:** The first task is to demonstrate, through simulation, and experimentally, Cu interconnect lines is inherently superior to Al metal lines in resisting ESD damages. It is our goal to show that, for the same ESD metal line width used, Cu designs provide higher ESD performance level; while for a specific ESD compliance level (*i.e*., 2KV or 4KV), narrower Cu lines are required compared to Al lines. There are three critical issues in conducting this task: First, one should be able to simulate the metal lines, in addition to simulating the semiconductor device structures as is normally done in TCAD simulation. Second, the metal lines and the underneath silicon structures should be simulated in combination, and simultaneously, so as to determine which part will be damaged during ESD events. Third, to demonstrate the goodness of Cu in this design, adequate silicon devices (structures and sizes) should be used to assure no damages in Si, so that the metal line (Cu & Al) induced ESD damage can be studied. To achieve this complex design task, a mixed-mode ESD simulation-design methodology developed in our laboratory was used that has the following features: First, direct coupling between electrical, thermal, device and circuit simulation that is the desired way to realize forward-oriented ESD design prediction. Second, simultaneously simulation of both metal lines and silicon structures underneath. The new ESD simulation methodology has been proven reasonably useful in predictive ESD design, although much improvement is still needed.

Design to show reduced ESD impacts on core IC by using Cu: The second design task is to demonstrate, by simulation and experiments, that the use of narrower Cu ESD metal lines helps to reduce ESD-caused IC performance degradation substantially as compared to using Al interconnects. Part I of this task is to design a multiple-stage oscillator, normally used to generate on-chip clocks, and using this high-frequency circuit to show how C_{ESD} may corrupt the clock signal as well as how Cu ESD design may recover such clock signal corruption. Part II

of this task is to illustrate broader impacts of C_{ESD} on IC chip. A low-power, high-speed, wide-swing, high-performance Op Amp circuit is designed for this purpose. The work is to show how C_{ESD} may deteriorate the Op Amp performance, such as, band width, slew rate, settling time, speed, driving capability and stability, etc. and then how well the Cu ESD design may recover such degradation substantially. Again, our goal is *not* to demonstrate how Cu interconnects may improve IC performance itself.

DESIGN

This work is designed for 1.5V applications. All ESD specifications are based on human body model (HBM) represented by the ESD failure threshold voltage level (ESDV) in kilo-voltage (KV). A complete ESD protection scheme with ESD protection units connected to each I/O pin is used according to UMC ESD design rules[2] and the common industrial practice[4]. The parasitic capacitive side effect of ESD protection devices on the core circuit being protected is simulated by connecting the ESD loads, C_{ESD}, to the proper I/O pins in simulation. Comparison data analysis is then conducted for the circuits with and without the C_{ESD} load to investigate the interactions between the ESD units and the circuit protected.

A. **ESD Protection Structures**.

Since the goal of this work is not to design novel ESD structures, instead, is to illustrate the negative impacts of ESD parasitic capacitance, C_{ESD}, on core IC circuits, we chose to use the conventional CMOS ESD protection structures, as suggested by UMC[2]. In fact, the large size of this type of ESD structure, hence more C_{ESD}, helps to illustrate the ESD influence on circuits in this work.

Although the CMOS ESD structure was chosen for this work roughly following the UMC ESD DR rules, we did make some modification because of the following consideration: First, the ESD effects must be studied via simulation as requested by the design contest rules. This ESD simulation work was conducted by use of our new ESD simulation methodology. Second, according to our simulation work as well as the industrial experiences, the UMC ESD DR rules represent a very conservative design guideline. Per our conversation with UMC as well as our knowledge of the current ESD design practices across the industries, we believe that there is much room to improve from the UMC rules. For example, the 2KV/300um rule seems to be very conservative and is most likely based on ESD stressing tests, which did not provide insights on whether the silicon structures or the metal lines caused the ESD damages -- a subject to be studied by this work, plus adequate safety margin. In addition, the minimum source-contact-to-gate-spacing (SCGS) of ~ 0.36um seems to be based upon the existing industrial guideline. However, our simulation shows that in VDSM design, the rule of using minimum SCGS may cause ESD failures because of the heat distribution from the nearby channel. The above observations are supported by that fact that UMC uses the same ESD design rules for both 0.18µm Cu and Al technologies, a common industrial practice, which certainly does not indicate the desired ESD metal design optimization. In this work, different ESD device sizes are included in our design matrix according to the ESD simulation results.

The ESD target performance level used in this work is 4KV by using a larger ESD device, partly to make C_{ESD} bigger for better demonstration, and partly to address the current ESD trend.

The CMOS ESD structures (NMOS for I/O to Ground and PMOS for I/O to V_{DD}) are used

as grounded-gate MOS (GGNMOS) devices as illustrated in *Fig. 1*. To achieve the 4KV ESD specification, a multiple-finger GGNMOS (and GGPMOS) structure with 12 50um-long fingers is used in this work per UMC design rules[2]. The main source of ESD parasitic capacitance, C_{ESD}, considered in this work is the ESD metal line associated inter-layer capacitance, including metal-to-subtrate, inter-metals, as well as metal-to-poly-gate if such overlap exists. In constructing the whole chip, a pair of GGNMOS and GGPMOS ESD units is connected to each I/O pin per UMC design rules. An exception is that separate ESD units are also used for output pin, instead of relying on the output transistors as suggested, because the output transistors in our circuits are not adequate for 4KV ESD protection. The design of ESD metal lines and estimation of C_{ESD} are discussed in the simulation section in details.

B. **A GHz 15-Stage Ring-Oscillator**

It is certainly that the number one issue associated global interconnect is the extra RC time delay (t_{delay}) caused by the metal interconnects, which becomes a real concern in high-speed large chip design. It is unquestionable that C_{ESD} of the ESD structures contributes to the overall interconnect RC delay as well, which, in some case, may become a major contributor because of the very wide ESD metal lines used in normal designs to achieve high ESD performance levels. The common rule is that at least a 20um wide metal line should be used in ESD structures, as is suggested by UMC in the ESD Design Rules. Although there is no adequate supporting theory and it seems to be a very conservative rule of thumb, it is the dominating rule in current ESD designs. It is well known that copper interconnect can substantially reduce the RC delay induced by global interconnects as compared to aluminum interconnect, which will certainly be discussed by many other teams. Our team wants to show that ESD metal related C_{ESD} may substantially degrade circuit performance too, *e.g.*, corrupt the on-chip clock signals in high-speed and RF designs, and using Cu interconnect may greatly alleviate such C_{ESD}-related side effect.

A simple way to illustrate this $C_{ESD} \sim t_{delay}$ effect is to analyze a multi-stage ring-oscillator circuit. For this purpose, a 2GHz 15-stage ring-oscillator circuit was designed. The stage number and the delay time were chosen based on better demonstration and measurement consideration. Minimum size transistors (L=0.18um) were used to reduce the intrinsic parasitic capacitance; hence more clearly show the influence of C_{ESD}. *Fig. 2* shows the schematics of this ring-oscillator circuit with C_{ESD} connected as external capacitive loads. There were two major considerations in selecting the loading volumes. First, each I/O pin must be protected per the common industrial rules. Second, in a high-pin-count advanced chip design, the overall C_{ESD} may vary sizably. Two loading scenarios were therefore used in this work. Scenario I has a single C_{ESD} load only at the probing pin of the 15-stage ring-oscillator to demonstrate the *least* side effect. Scenario II has full C_{ESD} load by connecting a pair of ESD devices at each stage to emulate the high-pin-count situation. Meanwhile, this full-loaded option allows us to evaluate variant C_{ESD} effect in measurements by probing at different stages, therefore offers more insights into this problem. The simulation results are to be discussed in details later.

C. **A Low-Power, High-Speed Op Amp**

It is certainly that the time delay is not the only parameter affected by C_{ESD}, although t_{delay} is one of the most important factors in high-speed digital designs. Other circuit performance parameters, such as, bandwidth and slew rate, are also important specifications in mixed-signal and RF

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designs. To demonstrate such broad-range C_{ESD} *versus* performance relationship, a low-power, high-speed, wide-swing, high-performance Op Amp circuit, often used in RF wireless communication applications, was also designed and analyzed in this work. Again, our goal is not to show how Cu interconnect can improve the Op Amp circuit itself, instead, we will demonstrate how Cu ESD design may alleviate the unavoidable ESD-induced degradation.

The designed Op Amp schematics are shown in *Fig. 3*. The circuit topology features differential input, push-pull output stage for wide swing, level shift, capacitive compensation with active nulling resistor for better stability, and global biasing for low stand-by power consumption. Internal compensation capacitor C_c is used to assure adequate phase margin of at least 45°. The main design goal of this Op Amp includes high gain, low power, wide swing, large band width, high slew rate and short settling time, therefore high speed, and so on. I/O pins are protected by the ESD structures as per the design rules. This translates into an internal C_{ESD} load connected at each I/O pin.

SIMULATION & DISCUSSION

A. ESD Simulation

General approach: The simulation work in this project consists of ECAD simulation for circuit design and combined TCAD-ECAD simulation for ESD design using a new ESD simulation-design methodology. Although ESD protection design is important and getting more complicated, the dominating ESD design approach still follows the trial-and-error procedure. The major problem facing IC designers is the inability to predict ESD designs before running silicons. Although design rules normally offer some ESD design guidelines, however, they are neither optimized nor guaranteed in terms of ESD performance. For example, the same ESD design rules are shared by the UMC Cu and Al technologies that certainly does not reflect any optimization in metal design. To address this practical ESD design problem, our group developed a new ESD simulation-design methodology[5]. This TCAD-based mixed-mode simulation methodology combines TCAD and ECAD simulation together that includes process-device-circuit coupling, electro-thermal coupling, as well as static and transient simulation. In conducting ESD simulation, established ESD circuit models (*e.g.* HBM -- human body model) are used to stress the ESD protection sub-circuits and the ESD performance is investigated through numerical simulation that solve device physics equations, thermal equations and Kirchhoff equations self-consistantly. The transient ESD failure criterion is the melting lattice temperature of the device materials (silicon or metals). There is no assumption needed in this simulation. Comprehensive simulation calibration is required that makes it possible to predict ESD design before running silicons. One new addition to this methodology is an integrated semiconductor-metal simulation module that can simulate a complete silicon device to investigate the reliability issues (*i.e.*, ESD) in both silicons and metals, which makes it possible for us to investigate ESD performance variation between copper and aluminum interconnects in this contest. Description of this new ESD design methodology is beyond the scope of this report. The following discussion covers the simulation results using this new ESD design methodology. Since TCAD simulation is part of this work, however, the UMC process recipes are not available to this team due to the fairness competition policy, we chose to use a similar 0.25µm high-speed CMOS technology from another leading foundry as a dummy simulation deck for TCAD simulation for the process steps

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associated with silicons. But importantly, all the material parameters for metals are from the UMC 0.18μm 1P6M technology. We do not expect any substantial issues associated with this strategy due to the following reasons: First, this work focuses on comparison study of copper and aluminum interconnects and all related back-end material parameters are from the UMC process. Second, our study of a few leading commercial 0.18μm and 0.25μm technologies indicates strong similarity in front-end device structures. Third, this work does not intend to design any advanced Si ESD structures, instead, over-sized GGNMOS devices suggested by UMC DR book are used to assure that the silicon device will *not* be the limiting factor. Hence, the moderate simulation errors caused by the front-end process recipes should not influence the results of Cu ~ Al interconnects comparison study in this work. Nevertheless, the difference certainly exists and one should not attempt to use the Si-related data in practical ESD design using this technology. Finally, as long as reasonable matching can be demonstrated between simulation and measurement, it is easy to adjust the front-end simulation results later on.

Bare Si Structure Simulation*:* The first part of ESD design is the simulation of *bare* Si GGNMOS ESD devices used in this work, meaning without metals -- a common practice in TCAD simulation. The goal is two folds: First, it is necessary to study the performance details of the suggested GGNMOS ESD structures that is not available from the UMC DR books. Second, the results will guide us to design adequate (over-sized) Si devices in order to make the metal lines (Cu or Al) the limiting factors in ESD tests.

There are two sizes for the GGNMOS (and GGPMOS) ESD devices in this work targeting 2KV and 4KV, respectively, with the simulated cross-section shown in *Fig. 4*. Following the UMC ESD design rules, both LDD implementation and salicide steps are excluded from the ESD structures for better performance. Multiple-finger ESD structures with finger length of 50μm are used for better uniformity. According the design rules, 6 and 12 fingers are used for the 2KV and 4KV devices, respectively. Other critical dimensions include channel length of 0.33μm, minimum source-contact-to-gate-spacing (SCGS) of 0.36μm, and large drain-contact-to-gate-spacing (DCGS) of 2.15μm, based on the design rules. As shown in *Fig. 4*, no metal lines are included in simulation, which is the common TCAD simulation practice and represents a major drawback in such simulation. However, this is good for this portion of the work.

The ESD simulation includes both static and transient simulation with device-circuit and electro-thermal couplings. Example transient ESD simulation curves are shown in *Figs. 5 & 6* for a 4KV-passed case and a 2KV-failed case, respectively, with *a* to *d* showing four typical characteristics: transient I~V curve, V~t curve, maximum lattice temperature T_{max}~I curve, and T_{max}~t curve, accordingly. The maximum lattice temperature (T_{max}) in the silicon device was extracted during simulation that was compared with the pre-set ESD failure criterion, the Si melting temperature of T=1966 °K in this work. Although there is still argument regarding the appropriate ESD failure criteria in simulation, the melting temperature seems to be the reasonable one so far. In *Fig. 5*, one can observe how the ESD device was triggered off and driven into deep snapback during an ESD pulse to form a discharging path, as well as how the T_{max} increases as the pulse current and time increase and then decreases after reaching the peak of the ESD pulse. In contrast, *Fig. 6* shows how the T_{max} grows up monotonically until reaching to the point of

$T_{melting}$ = 1966 °K, where the ESD device fails. *Figs. 7 & 8* shows 2D and 3D contours of the T_{max}, indicating the thermal defect occurs at the corner of the drain junction in agreement with the common understanding. The following critical parameters were extracted from the ESD simulation that are crucial to ESD design prediction: triggering voltage V_{t1} ~ 4.7V and triggering time t_1 ~ 0.08ns. From the ESD simulation, ESD device sizes of 56μm and 111μm are needed for 2KV and 4KV ESD protection. These numbers are clearly much smaller than that given in the UMC ESD DR book due to three reasons: First, this simulation uses a dummy process recipe. Second, industrial DR books are normally very conservative with over-sized safety margins included; however, they are not based on ESD simulation directly. Third, and most importantly, no calibration was included in this ESD simulation yet, which requires test chip data. This difference was taken into consideration in the ESD metal line design as will be discussed in the following section. The simulation data are listed in *Table I*.

Table I ESD simulation data for bare Si devices

ESDV	V_{t1} (V)	t_1 (nS)	Pass-width
2KV	4.70	0.080	56 (μm)
4KV	4.70	0.079	111 (μm)

***Individual ESD Metal Line Simulation**:* The center part of this work is the comparison study of ESD performance and C_{ESD} side effects in using Cu and Al interconnects. A newly developed *combined silicon-metal ESD simulation method* was used to conduct such investigation. The critical material parameters for copper, aluminum and dielectric layers used in this work come from UMC DR books and other references[6], which includes mass density, specific heat, thermal conductivity, melting temperature, resistivity, permittivity, and so on. These parameters are summarized in *Tables II & III*. This section discusses ESD simulation results of stand-alone metal lines that describe how the metal itself behaves during ESD events. The complete ESD structures (Si + metals) will be discussed in the next section.

Table II IL thickness and dielectric for C_{ESD} estimation

From	To	Thickness (KÅ)
Metal 1	Diffusion	10
Metal 1	Sub-strate	14
Metal 1	Poly-1	8
Metal 1	Metal 2	5.7
ILD-layers	ILD-films	ε
STI	SiO2	3.6
ILD	Si3N4	7
MD1	SiO2	3.6

Table III Critical parameters for ESD simulation

Material parameters[6]	Al	Cu	Si
Melting -Temp. (°K)	933	1357	1693
Density, ρ (Kg/cm^3, x 10^{-3})	2.7	8.96	2.32
Specific heat, C_p (J/Kg•°C)	899.6	385	850.9
Thermal resist. κ (W/°C•cm)	2.212	4.01	33.3
Resistivity, ρ (μΩ-cm)	3	2.7*	--

* From UMC DR.

In simulating the stand-alone metal ESD performance, single metal lines were created by TCAD and transient ESD simulation was then conducted for such metal lines. *Fig. 9a* shows a simulated single metal line sandwich structure with the metal layer (Cu or Al) covered by silicon and dielectric layers to simulate real-world operation. Based on the ESD design rules, the metal line length used is 20μm. Proper ESD pulses were applied to the two electrodes at the opposite ends of the metal line for ESD simulation. The melting temperatures of the metals ($T_{melting}$ = 1357 °K for Cu and $T_{melting}$ = 933 °K for Al) were used as the ESD failure criteria of metals. Transient T_{max} of the metal line was extracted during simulation. By comparing $T_{melting}$ with T_{max}, one will be able to determine how wide a metal line is required to pass a specific ESDV level, or, how high an ESDV level can

be achieved using a certain wide metal line in designs. All six metal layers (M1≈M2, M3≈M4, M5≈M6 from the DR) were included in the ESD simulation. *Fig. 9b* shows how the current flows along the metal line simulated during ESD events. A group of typical ESD characteristic curves for Cu and Al metal lines that passed or failed 4KV ESD stressing are shown in *Figs. 10 & 11*. Similar to the bare silicon simulation results, detailed I~V, V~t, T_{max} ~I, and T_{max}~t curves provide insights into how the metal lines behave during an ESD event. The simulation results are summarized in *Tables IV & V*. The maximum current density values from the UMC design rules for ESD, DC and AC metal electromigration are also included in the tables for comparison purpose, although there is no direct relationship between the electromigration data (life time tests) and ESD data (catastrophic failures). In the corresponding graphic representations, *Fig. 12a* shows good match among the maximum sustainable ESD current density levels (J, A/μm^2) *versus* metal layer curves for both Cu and Al under 2KV and 4KV ESD stressing. The observed subtle difference of the J~layer curves between metal layers may be attributed to different metal thickness and dielectric layers. Nevertheless, as shown in *Fig. 12b*, the trend from the ESD simulation is very similar to that extracted from the AC electromigration design rules and ESD design rules. It is easy to understand the substantial difference between the ESD simulation curves and the DR-extracted curves exists. First, there is no direct relationship between the ESD stressing and lifetime testing. Second, the ESD simulation was not calibrated yet and the ESD design rules seem to be very conservative that were optimized for metals.

Third, the data from the DR books are for 80 °C operation. In fact, using such current compliance data from the DR books, one may conclude that 223μm of Cu line would be needed for 2KV ESD protection, which is certainly incorrect even using the most conservative design strategy. In fact, this is one propelling reason for us to develop a novel ESD simulation methodology for ESD designs.

Table IV Maximum sustainable current density J(A/μm^2) of metal lines obtained from ESD simulation

M	Approach		Cond-itions	Max I-density, J(A/μm^2)		
				M1,2	M3,4	M5,6
Copper	Simulation		2KV	0.636	0.706	0.377
			4KV	0.636	0.706	0.323
	UMC	EM DR	DC[a]	0.017	0.022	0.020
			AC[a]	0.057	0.050	0.020
		ESD DR[e]	2KV	0.190	0.167	0.067
Alumi.	Simulation		2KV	0.448	0.391	0.226
			4KV	0.418	0.391	0.251
	UMC	EM DR	DC[a]	0.006[b]	0.006[c]	0.006[d]
			AC[a]	0.042[b]	0.035[c]	0.023[d]
		ESD DR[e]	2KV	0.190	0.167	0.067

[a] @ 80 °C per the UMC DR for metal width > 10μm. No RT data.
[b] For Al metal 1.
[c] For Al metal 2-5.
[d] For Al metal 6.
[e] Cu and Al technologies share the SAME ESD design rules!

Table V ESD simulation data: metal width required

Metal Layers	Metal line width needed, *W* (μm)		
	Al	Cu	***D**W* :Al →Cu
	2KV		
M1, 2	7	5	-28.6%
M3, 4	7	4	-42.9%
M5, 6	5	3	-40.0%
	4KV		
M1, 2	15	10	-33.3%
M3, 4	14	8	-42.9%
M5, 6	9	6	-33.3%

The most important observation from the ESD simulation results, as indicated by *Table V*, is that this simulation clearly shows that substantially narrower Cu metal lines are needed to survive the same ESD stressing levels compared to using Al metal lines. On the other hand, it indicates that much higher

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ESDV level can be achieved by using the same width of Cu interconnect. Such results quantitatively predicted that Cu interconnect is superior to its Al counterpart in ESD performance (30% -- 40% improvement). This also indicates that the C_{ESD}-induced circuit deterioration can be significantly reduced by using Cu interconnect. Such observation is the objective of this work, which is to demonstrate that the Cu interconnect technology can substantially improve ESD performance and reduce the ESD-induced circuit performance degradation, simultaneously. The simulated temperature distribution maps under ESD stressing are shown in *Fig. 13*, with *a & b* illustrating a localized case and a uniform heat dissipation case. At this moment, there is not a convincing explanation toward the different simulation mapping. It may be associated with the initial conditions in the numerical simulation. Nevertheless, it seems to be a good emulation of the practical ESD operations where thermal failures in metals are always localized phenomena.

***Simulation of Si Structure + Metals**:* With the previous discussion on ESD simulation of bare Si GGNMOS and stand-alone Cu/Al metal lines, it is ready to further investigate operation of a complete GGNMOS ESD device under ESD stressing. Integrated-mode ESD simulation of full GGNMOS structures, including Cu/Al metal, was conducted to study ESD operation of a real device. *Fig. 14* shows a sample complete GGNMOS structure with metal lines used in ESD simulation. According to the UMC design rules, Metal 1 was used. Inter-layer dielectric (ILD) materials and their thicknesses were selected from the design rules. Minimum source/drain metal length of 20μm was chosen according to UMC ESD rules. The above set-ups assure a real-world ESD structure being used in this simulation. Both Cu and Al interconnects with different metal line widths were simulated in which HBM ESD pulses were applied to the source and drain terminals with the gate grounded. Both static and transient ESD simulation was conducted in this work. In addition to normal I-V characteristics, maximum temperatures (T_{max}) of Si device, source/drain contact plugs, and source/drain metal lines were extracted during ESD simulation, separately. These extracted T_{max} data were compared with the melting temperatures for different parts of the device ($T_{melting}$ = 1966 $^{\circ}$K for Si, $T_{melting}$ = 1357 $^{\circ}$K for Cu and $T_{melting}$ = 933 $^{\circ}$K for Al) to determine where the ESD damage occurs during an ESD event. Since the goal of this work is to investigate the relative ESD performance of Cu and Al interconnects, the complete ESD protection structures were designed with large dimensions of Si structures so that the metal lines would be the weak link in ESD stressing. In studying the metal thermal damage, two heating sources must be taken into consideration: The first one is the distributed heat from the nearby Si channel junctions, which is normally considered in design practice and the SCGS/DCGS values in design rules are normally set based upon such consideration. The second, maybe more important, heat source is the metal self-heating due to *Joule* heating. The novel ESD simulation approach used in this work covers both type of heating sources in ESD simulation. It is worth to point out that, in reality, the metal lines inside a device may not fail immediately upon reaching the $T_{melting}$. It usually takes more heat to blow out the inter-layer dielectric materials to cause the metal failure. Experimental calibration is certainly necessary to better understand this issue. Nevertheless, this factor would not affect this work because the objective is to investigate the *relative* performance of Cu and Al interconnects.

A group of typical I-V characteristics of sample ESD structures with Cu and Al

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interconnects are shown in *Figs. 15 - 18* for variant metal widths and ESD pulse levels under both static and HBM transient ESD stresses. To better illustrate the T_{max}-distribution, the shown figures are selected from the cases in which ESD device failed the ESD stressing.

Figs. 19a-d clearly show the situation of a Cu device under a HBM transient ESD pulse where the Cu metal line was damaged. It is clear that *Joule* heat of the metal line, instead of the distributed heat from the Si channel heat source at the drain junction, caused the metal damage in this case. *Fig. 20* , from another Cu ESD sample device, shows how the distributed heat from the Si channel heat source at the drain junction may also heat up metal contacts at the source end and leads to metal failure eventually. This is the reason for using a large DCGS dimension as suggested in UMC ESD design rules (common practice). Another new, but very interesting, observation is made from *Figs. 21a-c* that illustrates how the distributed heat from the Si channel at the drain junction may also heat up the metal contact at the *source* end in a short channel device. This is an important phenomenon because all existing industrial ESD design rules suggest *minimum* SCGS dimension and large DCGS dimension. The latter rule may ensure higher ESDV level by preventing the drain metal from being heated up substantially by the junction heat source at the drain. While the former rule is normally used to reduce the series resistance associated with the source junction under the assumption that the heat generated at the drain junction does not affect the source metal substantially. However, the new observation indicates clearly that, in very deep sub-micron (VDSM) design, the minimum SCGS rule may not be used because the metal contacts at the source can also be heated up significantly by the heat source at the drain junction in Si channel. This phenomenon certainly deserves further study to assure better ESD designs in VDSM applications. An even clearer illustration of the metal line thermal damage during ESD stressing is shown by a 3D T_{max} contour map in *Fig. 22*, where high T_{max} was observed along the metal line, at the gate oxide location, and at the drain junction in the channel. Therefore, ESD damage may occur at any of these locations. The data obtained from this complete ESD device simulation agree with that from the single metal line simulation reasonably well.

To summarize, data from the ESD simulation show that the Cu interconnects performs superior to its Al counterpart in ESD operation. On one hand, 30-40% reduction in the metal line width when using Cu was observed for a specific ESD performance level compared to using Al, which translates into substantially lower ESD-induced parasitic capacitance (C_{ESD}) that may degrade circuit performance in high-speed designs. On the other hand, using the same metal line width, significant higher ESDV level can be achieved by using Cu metal lines compared to using Al interconnect. The benefits of such reduced ESD influences on core circuits in using Cu interconnect will be discussed in the following sections through a couple of functional circuits.

Estimation of C_{ESD}: Accurate estimation of the ESD metal related C_{ESD} is an important task in this work. It is certainly that using different metal layer will lead to variant overall C_{ESD}. In this work, metal 1 (M1) layer was used for primary ESD metal lines as per the UMC rules, with metal 2 (M2) used for bridging interconnection. Depending on the layouts, the total C_{ESD} includes the following capacitances: M1-to-substrate, M1-to-Diffusion, M1-to-Poly 1, and M1-to-M2. The data for inter-layer dielectric thickness and dielectric permitivity (ε) were provided by the UMC DR book and are listed in *Table II*. In calculating C_{ESD}, both the half-ESD-

protection, with one GGNMOS device connected from I/O to GND, and the full-ESD-protection, with a pair of GGNMOS and GGPMOS connected from I/O to GND and V_{DD}, situations were considered. From previous discussion of the ESD simulation results, it was observed that 30-40% of ESD metal line reduction can be realized using Cu interconnect compared to using Al interconnects. To be conservative, a reduction factor of 30% was used in this work for ESD metal line design using Cu and Al. The target of ESDV level of 4KV was used. The estimated C_{ESD} data are summarized in *Table VI*, which were used in circuit simulation.

Table VI Simulated C_{ESD} for 4KV GGMOS: Al ~ Cu.

GGNMOS	Cu	Al
Half-ESD C_{ESD} (pF)	0.150	0.214
Full-ESD C_{ESD} (pF)	0.300	0.429

B. Simulation of the ring-oscillator circuit

A 15-stage ring oscillator circuit, as shown in *Fig. 2*, is designed with proper ESD load connected to demonstrate how seriously the C_{ESD} of ESD units may affect the on-chip clock signal and how the Cu interconnect based ESD design can alleviate this problem as compared to its Al counterpart. Two ESD loading scenarios, single-loaded (1x C_{ESD}) and full-loaded (15x C_{ESD}), were considered in this work to simulate the least loading effect and the high-pin count loading condition. Simulated signal waveforms are shown in *Fig. 23* with delay time and frequency data listed in *Tables VII & VIII*. It is observed that C_{ESD} loading dramatically reduced the clock speed by ~70% (Cu) to ~80% (Al) for single-loaded and up to 98% for the full-loaded cases for the oscillator circuit studied. Such influence may cause clock signal corruption in some applications. It also shows that use of Cu interconnect technology can alleviate such performance deterioration problem significantly (~8%) and recover the clock signal substantially (~31%). This proves that use of advanced Cu interconnect technology cannot only improve ESD performance but also reduce the negative influences of the ESD units on core circuits substantially.

Table VII Influences of C_{ESD} on a 15-stage ring-oscillator circuit: Cu ~ Al.

Metals	Cap-load	C_{ESD} (*p*F)	t_d (nS)	*f* (MHz)
No ESD	Original	0	0.431	2320
Al	Single load: 1xC_{ESD}	0.43	2.079	481
Cu		0.30	1.578	633.7
Al	Full load: 15xC_{ESD}	0.43	44.75	22.35
Cu		0.30	31.37	31.88

Table VIII Speed degradation *w.r.t.* the original clock frequency due to C_{ESD}: Cu ~ Al.

ESD load	Original (no ESD)	Al	Cu
Single ESD load	0	-79.27%	-72.69%
	Al to Cu Improvement	→ +31.75% →	
	Reduction in degradation	→ +8.3% →	

C. Simulation of the Op Amp circuit

A low-power, high-speed, wide-swing Op Amp circuit was used to demonstrate the broad influences of parasitic C_{ESD} on overall performance of a functional chip. The circuit schematics are shown in *Fig. 3*, with the ESD loading effect represented by C_{ESD}. The target specifications of the circuit are the following: V_{DD}=1.5V; very low power consumption of 0.47 mW; gain of 74dB; phase margin of 61°; unity-gain band-width of 156 MHz; -3dB band-width of 34 KHz; wide swing of 0.96V measured at 80% small-signal gain, very high slew-rate of 215 mV/nS; and very short settling time of 5 nS measured at 1% of the output. These data are summarized in *Table IX*. External load (C_L) of 1 pF was used for these data.

Simulation with different C_{ESD} for both Cu and Al interconnect was conducted. *Figs. 24-27* show the gain Bode plot, phase Bode plot,

large-signal step response for slew-rate and small-signal step response for settling time measurements, with the related data summarized in *Table X & XI*. It is clear that the ESD loading, C_{ESD}, can substantially deteriorate performance of the high-speed Op Amp, *i.e.,* over 24% deterioration in unity-gain band-width for Al circuit (~18% for Cu), ~15% degradation in slew rate for Al circuit (~11% for Cu), and ~57% increase in settling time for Al (~45% for Cu). All the above parameters are critical in high-speed operation. Compare the Cu circuit with its Al counterpart, it was found that substantial reduction (~≥20%) in the performance deterioration of the circuit was realized by using Cu interconnects, which translates into significant improvement in circuit performance.

To summarize this portion of the simulation work, the important observation is that, while higher ESD specifications is in demand; parasitic effects from the ESD protection units used may dramatically affect the core circuit being protected. However, compared to Al technology, use of Cu interconnects can improve ESD robustness and reduce the ESD-induced circuit performance degradation simultaneously, in addition to achieving higher circuit performance.

Table IX The Op Amp circuit specifications

Technology	0.18um, 1.5V, Cu, 1P6M
Power supply (V)	1.5
Gain (dB)	74.21
Phase margin	62.2°
f_T (MHz)	156.5
f_{-3dB} (KHz)	33.9
V-swing (V, @80%)	0.96
Settling time (ns, @1%)	5.01
SR (mV/nS)	215.6
Power cons. (mW)	0.469

Table X Influences of C_{ESD} loads on the Op Amp circuit: Cu ~ Al, (C_L = 1*p*F).

ESD	C_{ESD} (pF)	*f_T (MHz)*	*Phase marg.*	*SR (mV/ns)*	*t_{set} (nS)*
None	0	156.5	62.2°	215.6	5.01
Al	0.3	118.8	59.9°	181.8	7.88
Cu	0.43	127.4	60.8°	190.7	7.28

Table XI Op Amp performance degradation due to C_{ESD} loads: Cu ~ Al.

Parameters	No C_{ESD}	Al	Cu
f_T (MHz)	156.5	-24.1%	-18.6%
		Reduction in Degradation	
		→ +22.8% →	
Phase Margin	62.2°	-3.7%	-2.3%
		Reduction in Degradation	
		→ +39.2% →	
Slew rate (V/us)	215.6	-15.7%	-11.5%
		Reduction in Degradation	
		→ +26.8% →	
t_{set} (nS, 1%)	5.01	-57.3%	-45.3%
		Reduction in Degradation	
		→ +20.9% →	

TEST PLAN

The Phase I simulation results are subjected to experimental confirmation in Phase II. The test plan of this work has two parts: design for test and measurement methods.

A. Design For Test

To prove the simulation results, A two-part experiment plan was developed to measure both individual ESD protection structures (Part one) and the circuits under the C_{ESD} influences (Part two).

Part one of the experiment is designed to investigate ESD performance of individual ESD protection devices and metal interconnects. There are three test sets designed for measurements: bare Si devices; metal lines fingers; and complete ESD devices. The ESD protection units (GGNMOS and GGPMOS) include both

single-finger and multi-finger structures. The first test set is for bare Si structure evaluation for which wide metal lines (>20μm) are used to assure no metal damage occurs, therefore, allows us to evaluate the silicon devices under ESD stressing. The second test set consists of single-finger metal line test patterns designed for investigating the detailed thermal reliability properties of metal interconnect in ESD events. Ideally, both Al and Cu interconnects should be included in the test patterns. However, this is not possible in this contest because the Al option is not provided by UMC. Nevertheless, this constraint will not affect the conduction of this work. Because the difference of ESD-induced negative impacts on core circuits when using Cu and Al can be reasonably emulated by using different metal line widths in the design. Based on the simulation, a variation factor of 30% in ESD metal width between Al and Cu was chosen. In fact, such strategy was chosen by all other teams in evaluating global interconnect capacitance. On the other hand, the absolute advantage of Cu over Al in ESD performance has been proven experimentally and qualitatively by other researchers[3]. The data of these ESD structures will then be used for simulation calibration in a practical ESD design otherwise. The third test set consists of the complete GGMOS ESD structures, same as that will be used on IC chips, designed to further study the metal performance under ESD stressing in real chips. For this reason, large Si device size (300μm) was chosen to ensure that the metals are the limiting factor in ESD events. This test pattern plan is summarized in *Table XII*.

Part two of the experiment is designed to study the interactive performances of ESD units and IC circuits using two sample functional circuits. The first circuit is a ring oscillator for which the test patterns include the followings: an oscillator circuit without ESD attachment for evaluation of the original performance; oscillator circuits with single ESD load (1x C_{ESD}) for evaluation of the least influence of a C_{ESD}; and oscillator circuits with full ESD loads (15x C_{ESD}) for emulation of the worst ESD loading case in high-pin-count cases. Both Al and Cu versions are included where emulation of Al design is realized by scaling up the ESD metal width by 30% from the Cu design according to the simulation results. The second circuit is a high-speed Op Amp for which the test patterns consist of an Op Amp circuit without ESD connection to study the intrinsic circuit performance and a pair of circuits with proper C_{ESD} loads for both Al and Cu to investigate the influences of C_{ESD}. The test circuits are summarized in *Table XIII*.

Table XII Summary of the test patterns designed for measurements of the individual ESD structures.

Type	Feature	Design Variables	
Bare Silicon device	Metal 1 >20μm	Finger #	1, 1+, 2, 2+, 3, 4, 5, 6, 7, 8
		Finger length (μm)	50, 56, 100, 111, 150, 200, 250, 300, 350, 400
Metal lines	Cu	M1 (μm)	3, 5, 7, 10, 12, 14, 17, 20
		M4 (μm)	4, 10, 14, 20
		M6 (μm)	3, 10, 14, 20
Full devices	Si size: 300μm	Metal 1 width (μm)	
		3, 5, 7, 10, 12, 14, 17, 20	

**Note*: 1+ & 2+ still use single finger, but longer (>50μm).

Table XIII Summary of the circuit test kits

Circuits	Test circuit features	
Ring Oscillator circuit	No ESD	0x C_{ESD}
	Al	1x C_{ESD}
		15x C_{ESD}
	Cu	1x C_{ESD}
		15x C_{ESD}
Op Amp circuit	No ESD	0x C_{ESD}
	Al	1x C_{ESD}
	Cu	1x C_{ESD}

With the above design for test, it will be possible to completely investigate the ESD robustness of Cu interconnect, negative ESD

influences on core circuits, and potential benefit of Cu technology in reducing such performance deterioration of the circuits.

B. Measurement Methods

The measurement methods for this work include the following test means:

Normal IC measurement of both the oscillator circuit and the Op Amp circuit, *e.g.,* waveform probing, large and small signal step function response study, and so on.

The first type of ESD measurement uses quasi-DC curve tracing techniques that provide such information as triggering voltage, holding voltage, on-resistance, etc. however, such data do not reflect real-would ESD events, which are transient.

A second ESD measurement method is to use a transmission-line-pulsing (TLP) technique that closely emulates real ESD stressing conditions. This transient testing method provides the following critical parameters: triggering voltage and current, holding voltage and current, thermal failure threshold voltage and current, etc. The TLP technique is the only available non-destructive ESD testing means. A Barth Model 4002 TLP tester will be used in this work.

Finally, to qualify the ESD performance of a chip, one must conduct ESD zapping tests using different ESD stressing model (*e.g.,* HBM model, etc.) following the industrial standards. This test reveals what ESDV level could be achieved and how robust an ESD design might be, although it offers no insights into how and why an ESD design operates in a specific way.

Based on the above test strategy and methods, comparison study of the simulation and measured data will be conducted to complete this work.

LAYOUT PLAN

The layout plan was made according to the test strategy described previously. The completed layout floor plan is shown in *Fig. 28*, where the upper portion consists of the ring-oscillator (*Fig. 29b*) and Op Amp circuits (*Fig. 29a*) while the lower part comprises all the individual ESD test structures, i.e., bare Si devices, single metal lines, and full ESD devices. A complete ESD I/O unit is shown in *Fig. 29c*. A 3.5mmx3mm die was used for this design. Since this chip has high bond-pad count, due to large set of ESD test devices, and operates at high speed, two QFP-100 packages were used to accommodate this chip.

MEASUREMENTS & DISCUSSIONS

Tasks: The measurement plan consists of two main tasks: *Task 1* is to conduct ESD tests using curve tracer and TLP (transmission line pulse) tester on all individual ESD test structures to confirm the simulation results – substantial less Cu metals are needed for the same ESD performance levels compared to Al interconnects, therefore significantly reduces the ESD metal induced parasitic capacitance C_{ESD}. *Task 2* is to measure the ring-oscillator and Op Amp circuits with different ESD protections to confirm the simulation finding that Cu indeed provides adequate ESD protection, meanwhile substantial degradation in circuit performance due to C_{ESD} can be recovered in using Cu as opposed to using Al.

Manufacturing Problems: Complete measurements cannot be conducted according to the testing plan because the circuits do not function due to **mis-processing**. Fortunately, part of the test patterns associated Cu interconnects (individual ESD testing structures) work properly, which makes it possible for us to conduct *Task 1* tests, therefore, partially confirm our simulation

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findings. This section covers measurement data and discussions for Cu interconnect test patterns only and a brief description for the debugging procedures. The complete die photo is shown in *Fig. 30*.

Measurement Results for Cu ESD Structures and Discussions: A group of metal line test patterns with specially tailored line widths (W=3µm, 5µm, 7µm, 10µm, 14µm, 16µm and 20µm) was designed for all Cu interconnect layers (M1 to M6) to investigate the optimized metal line width required for specified ESD performance levels in both Cu and Al in comparison with the traditional material-independent ESD design rules for metal interconnects. TLP testing was conducted for those Cu metal line test patterns with different widths. I-V curves were obtained for each test pattern in TLP testing. Leakage current measurements were conducted after each TLP pulse stressing to determine the failure threshold points of each Cu metal test pattern. ESD performance level data (*i.e.*, ESDV in KV) were extracted for various Cu metal line widths, which are compared with simulation data and the ESD Design Rule data.

The first important factor observed in measurement was that the thickness of the top two metal layers (M5 & M6) was about only half of the 1µm specified in the DR book. The actual thickness for M5&6 was about 0.56um according to the inputs from UMC. This number was used to adjust the previous simulation data in order to compare with the testing data meaningfully.

Fig. 31 shows the *maximum sustainable current per line-width* (representing ESD performance levels) *versus Cu metal width* from both simulation and measurements. It was observed that simulation agrees with testing reasonably well within a factor of about 2 for all six metal layers across a broad range of line-width. This indicates that the mixed-mode ESD simulation method used in this design works properly. The factor of 2 was then used to calibrate the previous simulation data for meaningful comparison with the measurements. This can be treated as a typical simulation calibration procedure to assure design prediction as discussed in the simulation section.

Data for *ESD performance levels versus metal line widths* as well as the *required metal line widths versus different metal layers* for 2KV and 4KV ESD performance are shown in *Figs. 32 & 33* for both simulation and measurements. Fairly good matching between testing and simulation was clearly observed for all six metal layers. The ESDV ~ metal width curves in *Fig. 32* shall also serve as a proven guideline for selecting adequate ESD metal line-width *rationally* in practical designs, as opposed to using the traditional *all-fit* 20µm ESD metal design rule.

Data for the *maximum sustainable current density* (representing ESD performance levels) *versus metal line-width* are shown in *Fig. 34* for Cu, Al and ESD design rule data from both simulation and measurements, which are summarized in *Table XIV*. The important observations follow: First, simulation shows much higher current handling capability of metal interconnects compared to the ESD design rule data. Alternatively, substantially better ESD performance shall be expected for metals compared to that indicated in most traditional ESD metal design rules. This remark is reasonable considering the fact that traditional ESD metal design rules are largely empirical and independent of interconnect materials and the ESD level desired (i.e., same rules for 1KV, 2KV, 4KV, etc). The most important derivation from this observation is that much less metal coverage may be needed for specific ESD performance in practical designs

– translating into substantially lower parasitic effects (C_{ESD}) associated with ESD protection structures. Secondly, it is clearly observed that significantly narrower Cu metal line-width is needed as opposed to that of its Al counterpart for the same ESD performance levels. Such observation and conclusion are the goal of this project. In summary, the simulation and measurement data clearly indicate that Cu interconnects may not only assure adequate ESD performance as compare to Al, but also substantially reduce the ESD metal induced parasitic C_{ESD}, therefore improve overall circuit performance.

Table XIV Maximum sustainable current density

J (A/um^2)		M1, 2	M3, 4	M5, 6
Cu	SIM*	1.720	1.189	0.939
	Test	1.722	1.192	0.934
Al (SIM)		0.448	0.391	0.226
ESD DR's		0.190	0.167	0.067

* Data adjusted to real metal thickness and calibration factor as discussed.

Measurements of Circuits: Unfortunately, no measurement can be conducted for the designed ring oscillator and Op Amp circuits because they are not functional due to mis-processing. This problem makes it impossible for us to argue that Cu indeed could reduce the degradation in circuit performance due to C_{ESD}, while achieve the same ESD robustness as compared with Al.

Debugging: A fair amount of work were done to find out the root causes of the circuit malfunction. Since none of the circuits seemed work in initial testing, particularly, resistive behaviors were observed in all initial testing, we re-checked our layouts and did not find any problems. We then measured I-V characteristics between any two bonding pads within the same circuit blocks and between different circuit blocks. Plain resistive I-V characteristics were observed in all cases. In conjunction with the fact that all metal test patterns including a group of inductors and transformers work properly, we suspected that global short-circuit through the substrate may be the problem. With the mask inspecting results from UMC, it was confirmed that no N+ layer exist, which means all NMOS transistors are essentially P-well resistors. This is the root cause to the circuit malfunction. What made this happen is fairly breath-taking: We did not draw any N+ layers because the UMC DR says that N+ layers can be generated *either* through Boolean function *or* by drawing, just like in the P-well and N-well case. However, we did not remove the N+ layer number (#32) from the sample tool form provided by UMC, which was actually used by UMC to create N+ layers – therefore, no N+ layer was physically generated in our silicon.

CONCLUSIONS

In conclusion, this work conducted a comprehensive investigation on the advantages of using copper interconnects in ESD protection designs. GGMOS ESD protection structures using Cu interconnects were designed with the target ESDV levels of 4KV. One 2GHz ring oscillator circuit and one low-power, high-speed Op Amp circuit were designed for comparison study. In Phase I, the simulation results show that, while ESD protection devices may inevitably affect circuit operation, the use of Cu technology can not only significantly improve the ESD robustness (> +30%) but also substantially reduce the unavoidable negative influences (~ +20%) of the ESD protection devices on the core IC chips being protected. In Phase II, the measurement results for individual Cu metal line ESD test patterns match the simulation data reasonably well. It was observed clearly that Cu has substantially better ESD performance compared with Al. Alternatively speaking, significantly narrower Cu line-

width is needed compared to Al for the same ESD performance level. This translates into substantially less ESD metal associated parasitic effect (C_{ESD}) on overall circuit performance in Cu technology as opposed to its Al counterpart. It was also observed that traditional ESD metal design rules are over-conservative. It was found that adequate, but substantial less ESD metal coverage may be needed in practical ESD design (for both Cu and Al cases), which offers substantial benefits in parasitic-sensitive high-speed IC designs. This work clearly demonstrates the benefits of using Cu interconnect technology in high-speed designs to realize both higher ESD robustness and lower ESD-related parasitic effects compared to the traditional Al interconnect technology.

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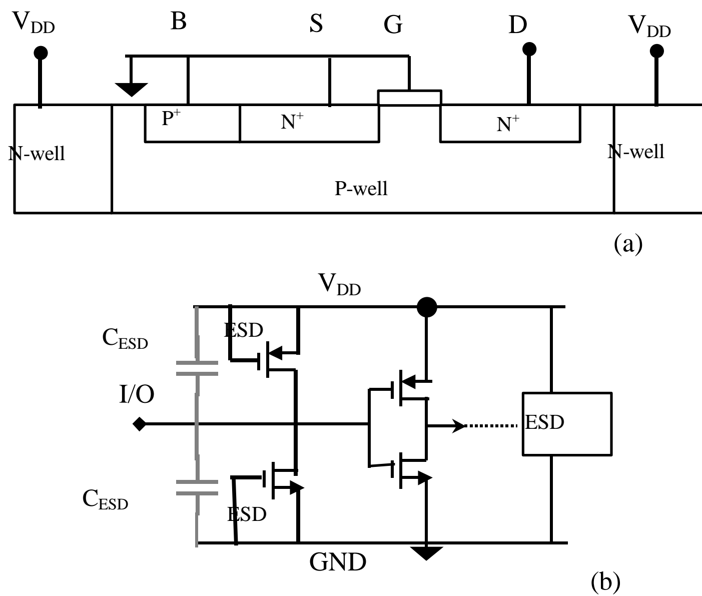


Fig. 1 GGMOS ESD protection structure: a) cross-section for a GGNMOS, b) a complete ESD protection scheme.

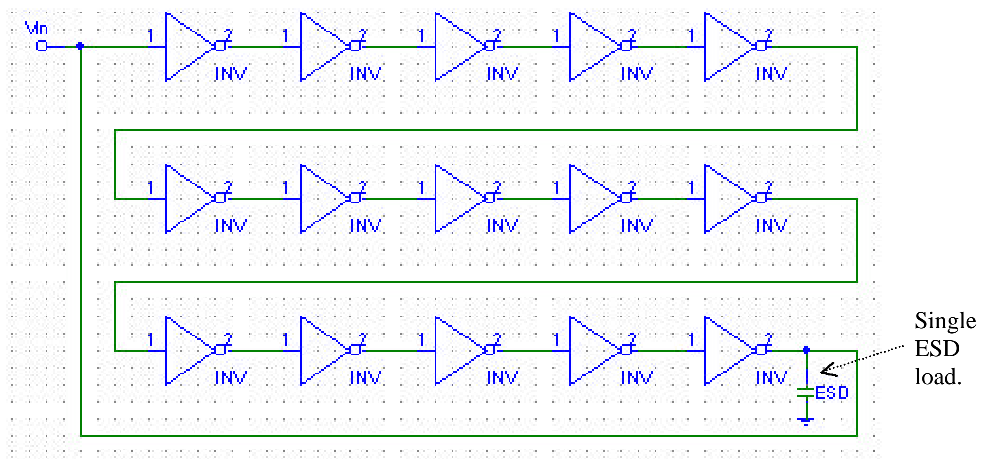


Fig. 2 Schematics of a ring-oscillator circuit. Parasitic capacitive side effects from ESD protection units are simulated by (single-load case) 1xC_{ESD} connected to the I/O pins. For full-load case, 15xC_{ESD} are at each probing node.

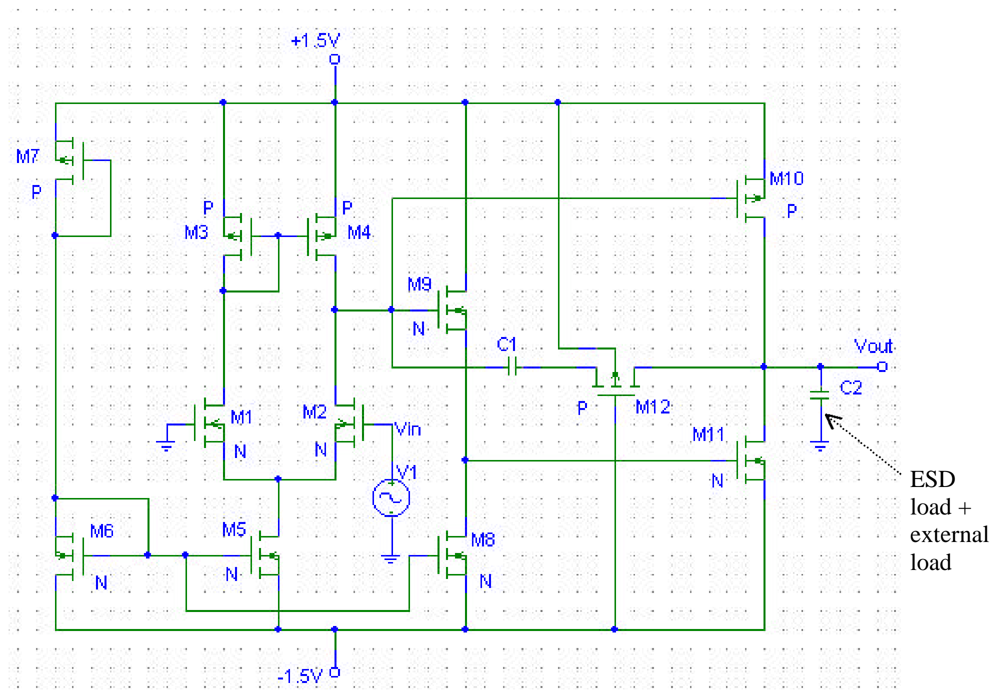


Fig. 3 Schematics of a high-performance Op Amp circuit. Parasitic capacitive side effects from ESD protection units are simulated by C_{ESD} connected to the I/O pins.

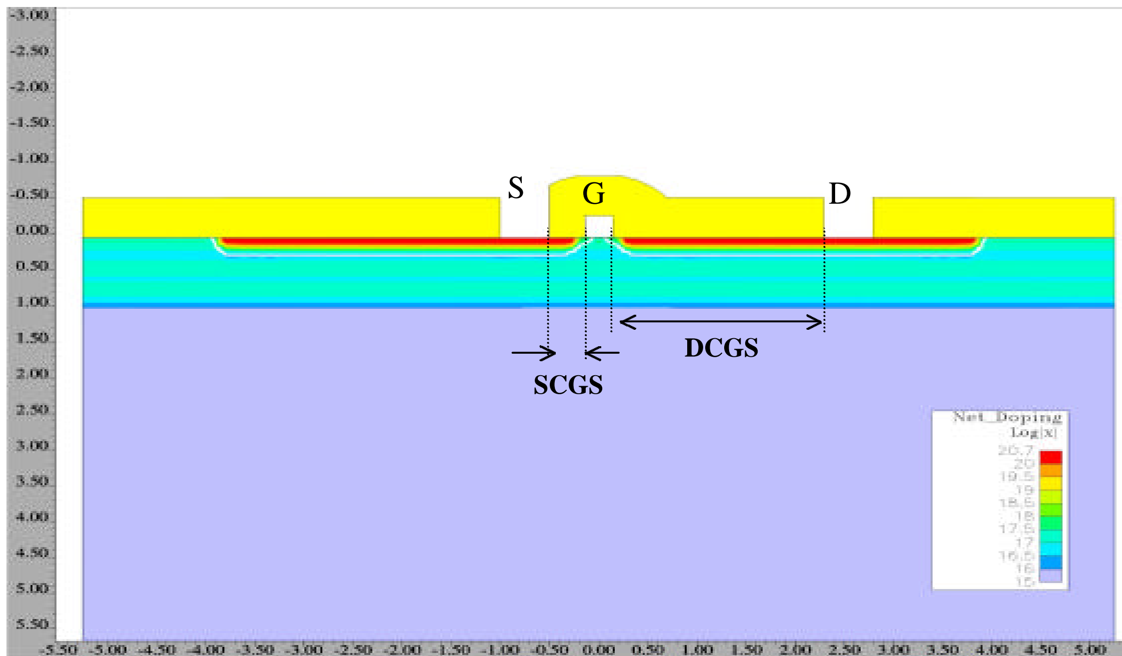
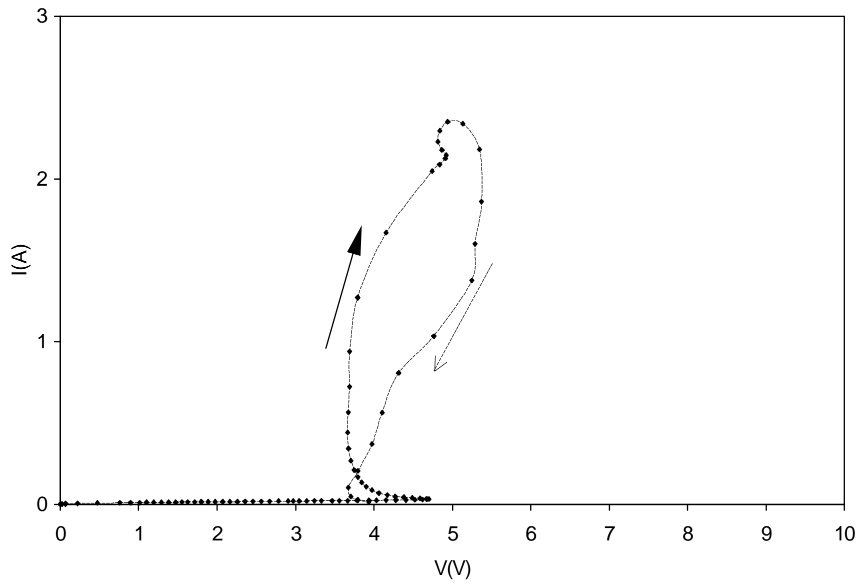
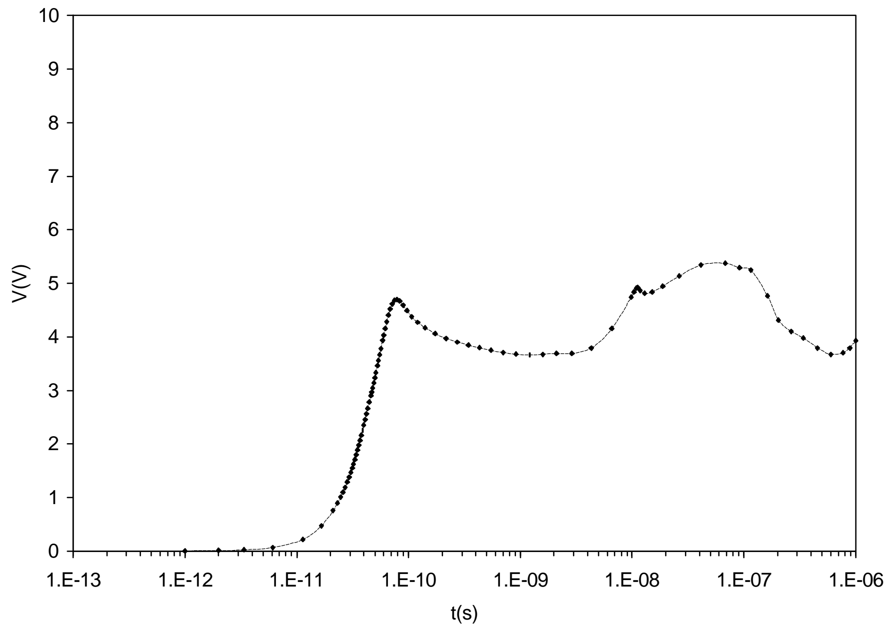


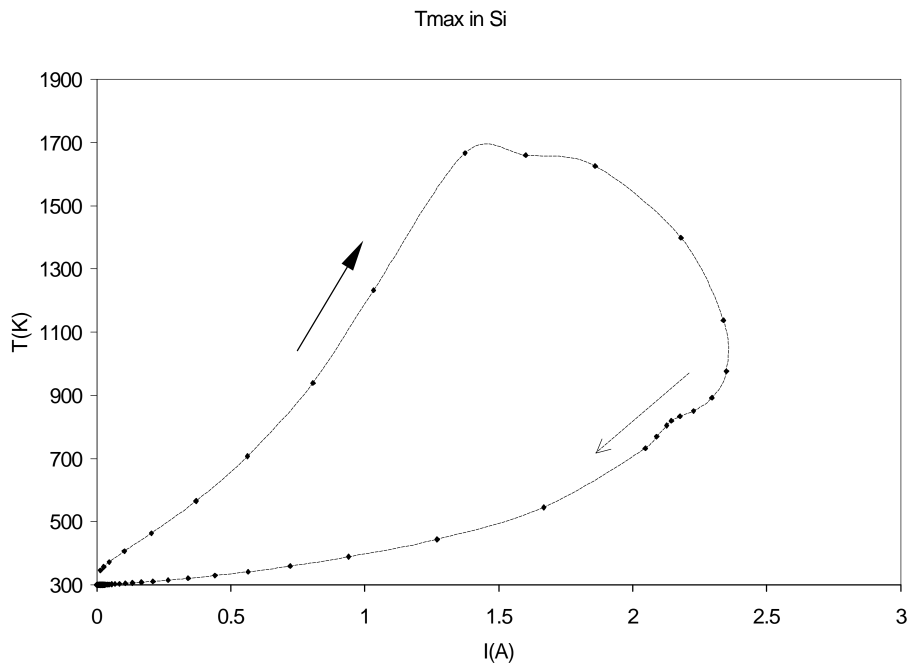
Fig. 4 Simulated cross-section of a GGNMOS ESD device without metal lines. Large lateral and vertical dimensions were used for realistic thermal distribution consideration.



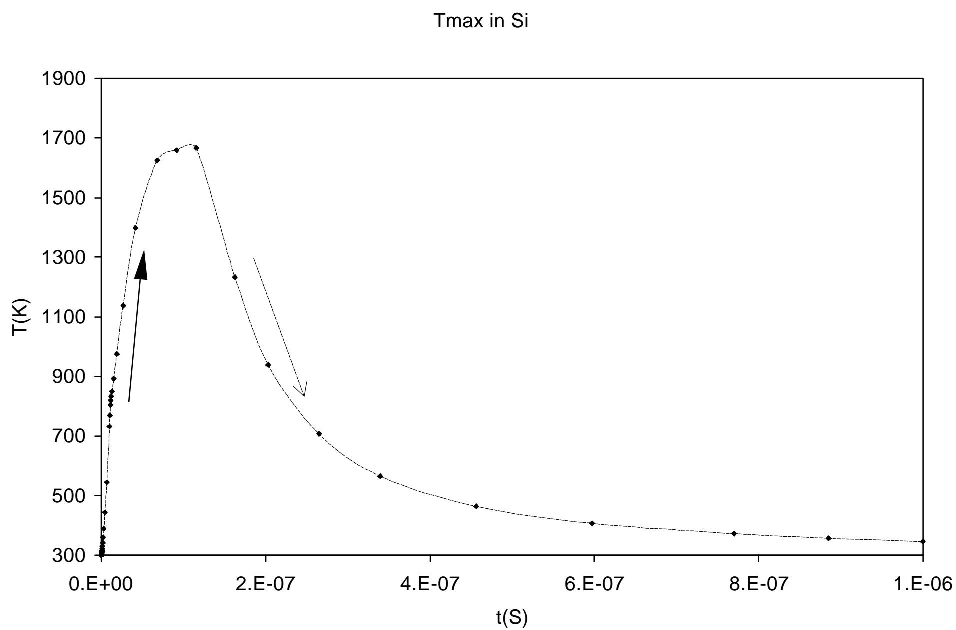
(Fig. 5a)
I-V curve during a HBM 4KV ESD pulse.



(Fig. 5b)
Time response during a HBM 4KV ESD pulse.



(Fig. 5c)
T_{max} ~ I curve during a HBM 4KV ESD pulse.



(Fig. 5d)
Transient T_{max} variation in Si during a 4KV ESD pulse.

Fig. 5 Transient ESD simulation results of a GGNMOS ESD protection device that passed HBM ESDV=4KV with a size of 111μm. Bare silicon structure.

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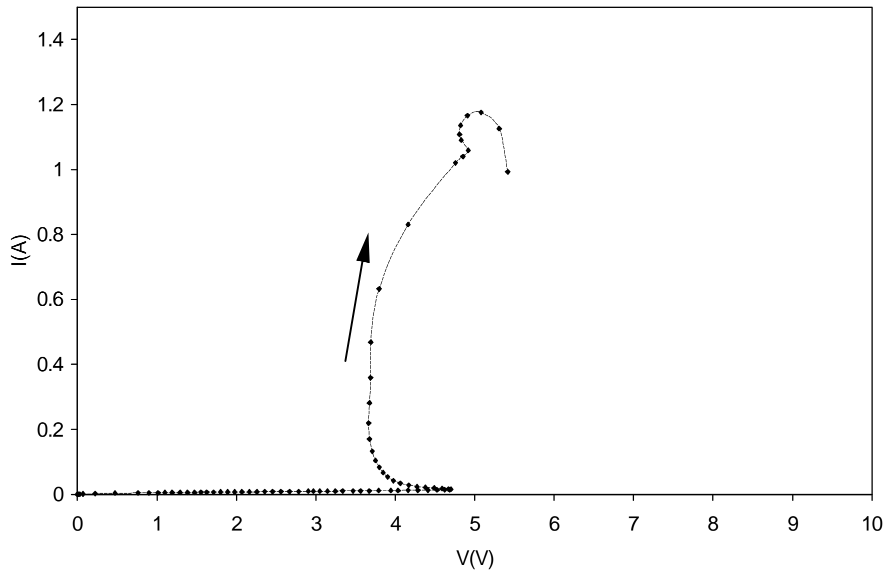
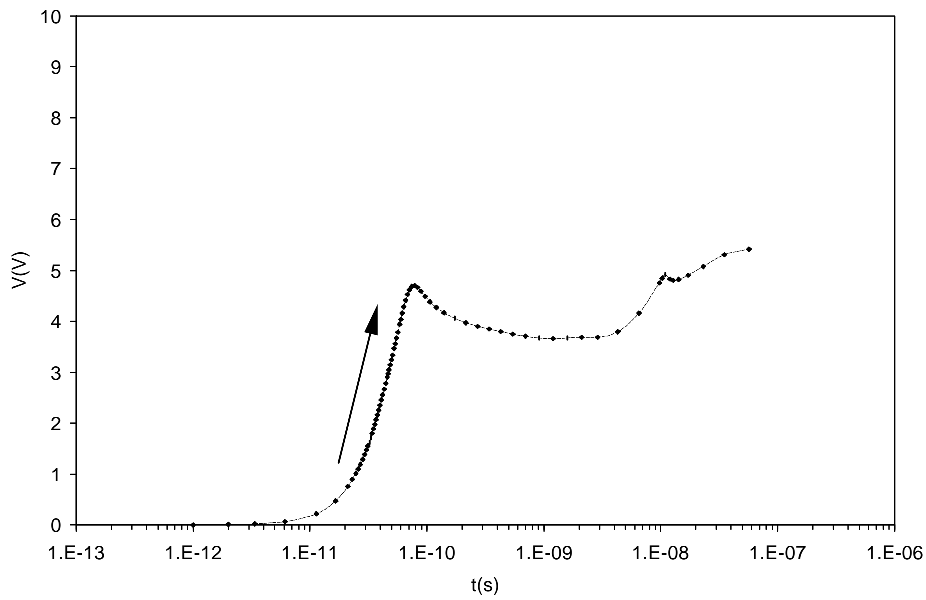
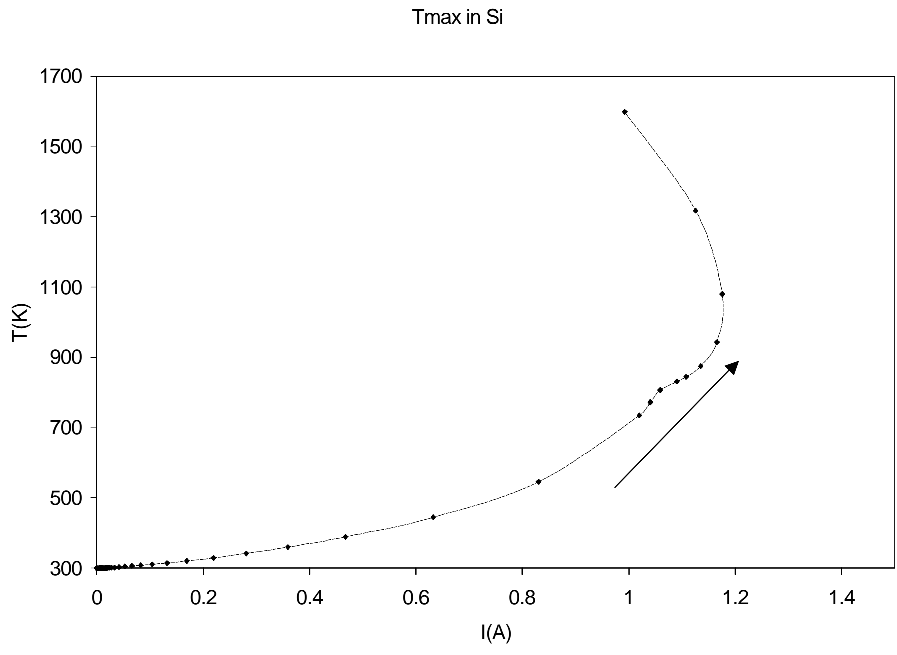


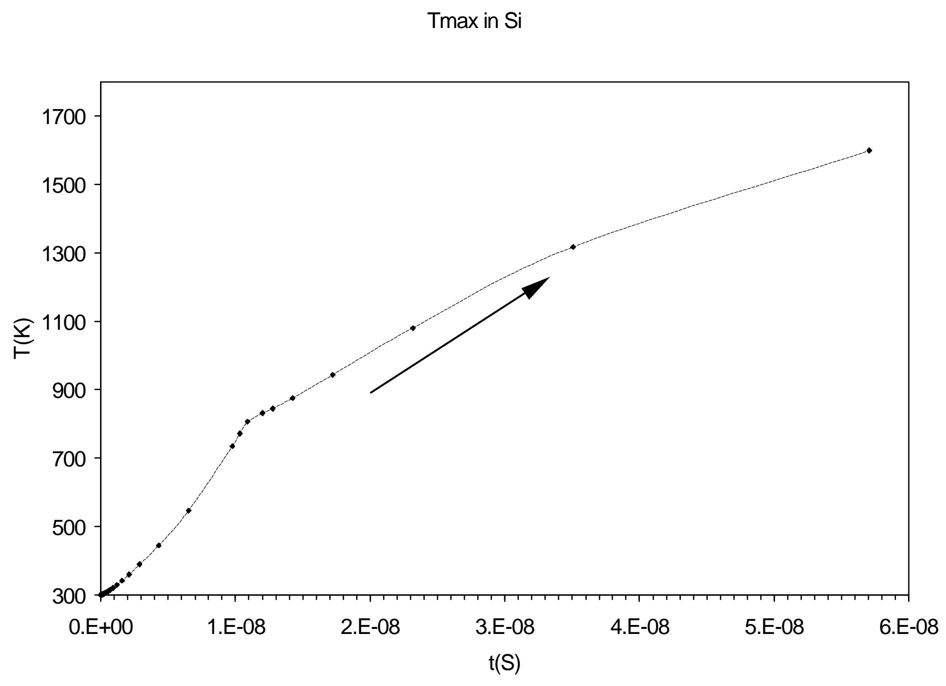
(Fig. 6a)
I-V curve during a HBM 2KV ESD pulse.



(Fig. 6b)
Time response during a HBM 2KV ESD pulse.



(Fig. 6c)
T_{max} ~ I curve during a HBM 4KV ESD pulse.



(*Fig. 6d)*
Transient T_{max} variation in Si during a 4KV ESD pulse.

Fig. 6 Transient ESD simulation of a GGNMOS ESD protection device that failed at HBM ESDV=2KV with a size of 55µm. Bare silicon structure.

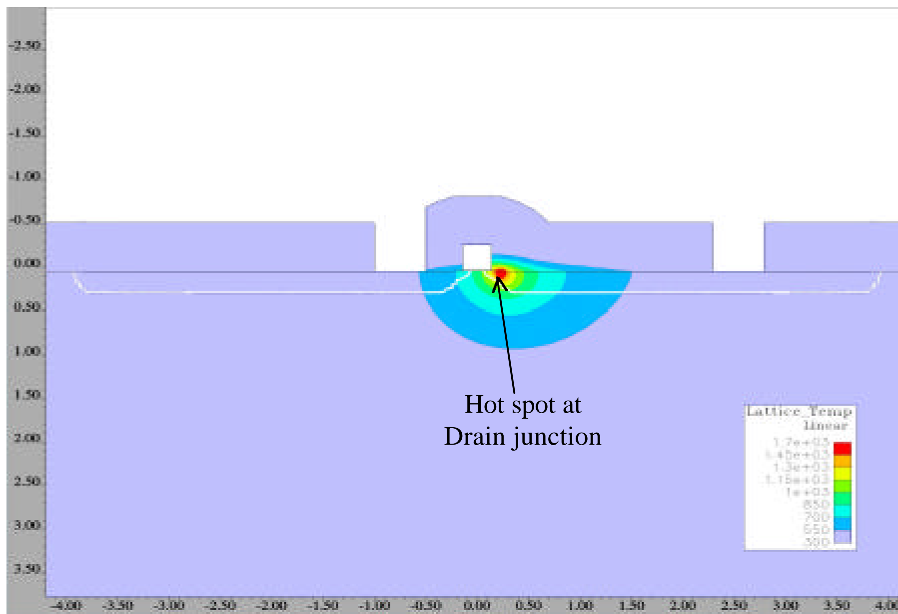


Fig. 7 Simulated T_{max} contour for a GGNMOS during ESD event shows localized thermal defect at the drain junction that causes ESD failure. Bare Si structure.

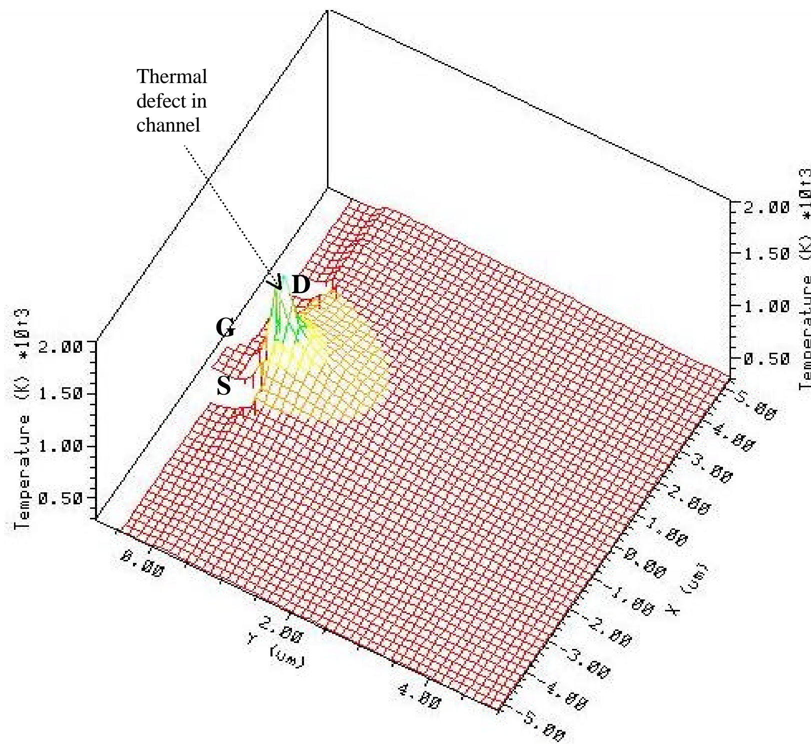


Fig. 8 3D T_{max} contour of a GGNMOS device during ESD stressing indicates localized ESD failure at the drain junction with insignificant temperature increases in metal lines. Bare Si structure.

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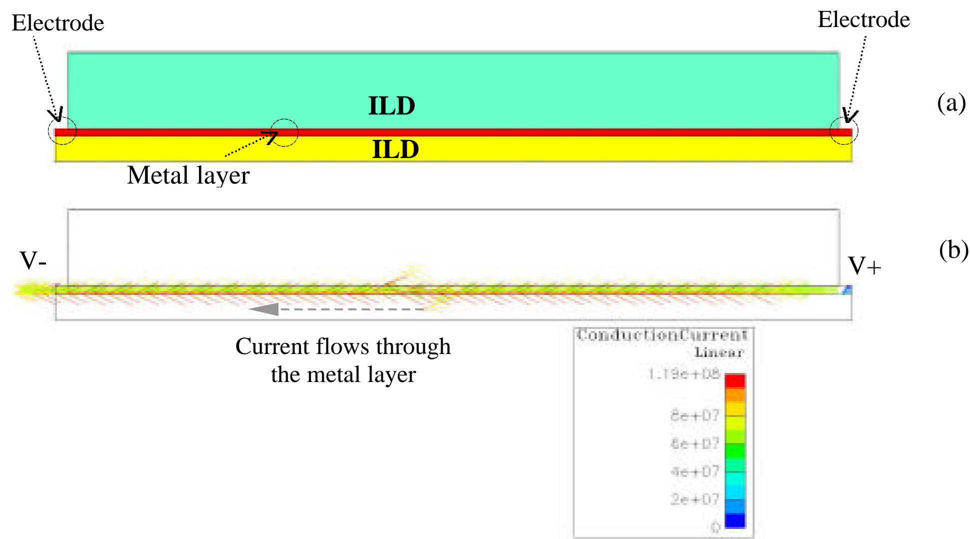
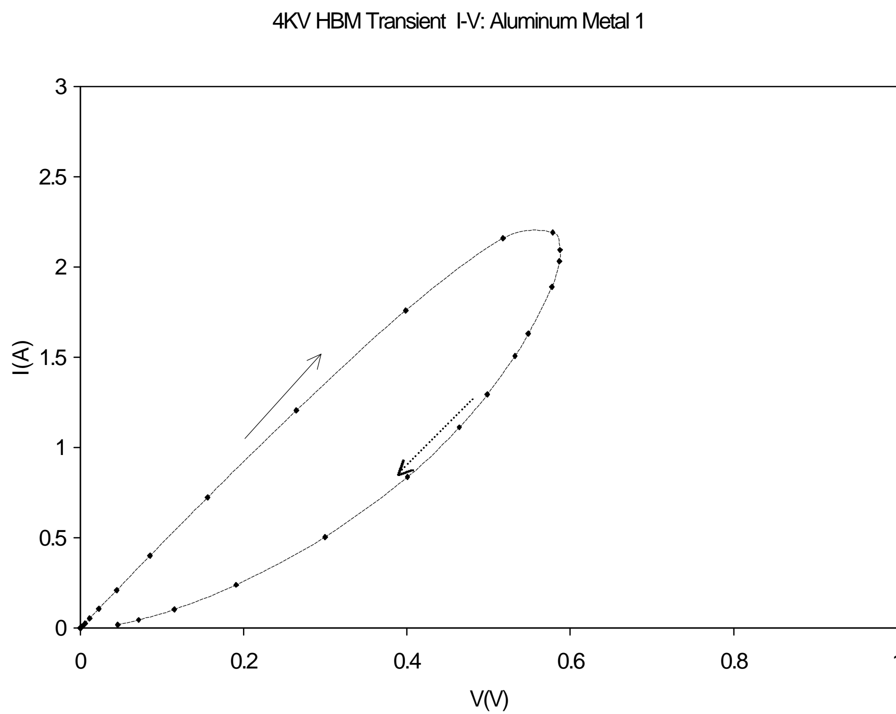


Fig. 9 a) A single metal line sandwich structure used for ESD simulation of pure metal lines. b) Current flow map within the metal line simulated during an ESD event. Stand-alone metal line for simulation.



(Fig. 10a)

I-V characteristics of a single Al metal line under 4KV transient ESD pulse.

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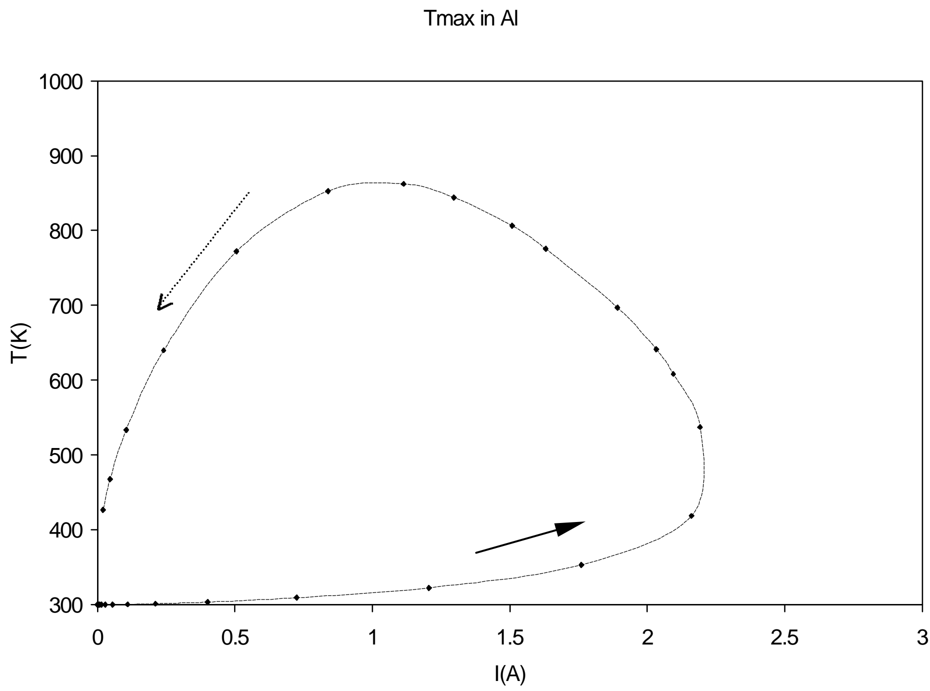
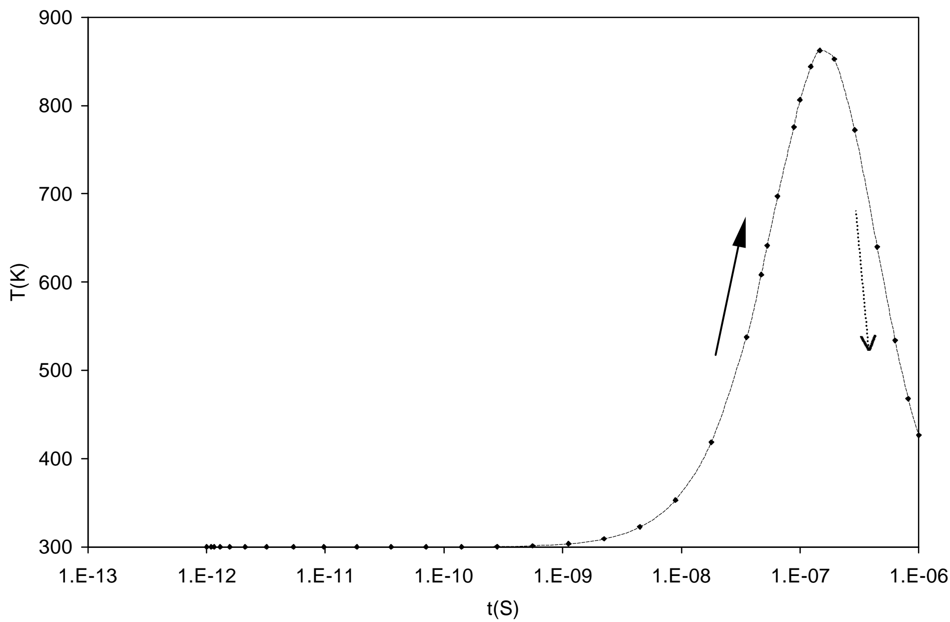


(Fig. 10b)
T_{max} ~ I curve during a HBM 4KV transient ESD pulse.



(*Fig. 10c)*
Transient T_{max} variation in the metal line during a 4KV transient ESD pulse.

Fig. 10 ESD characteristics of a single Al metal line that passed 4KV ESD test with a width of 15µm.

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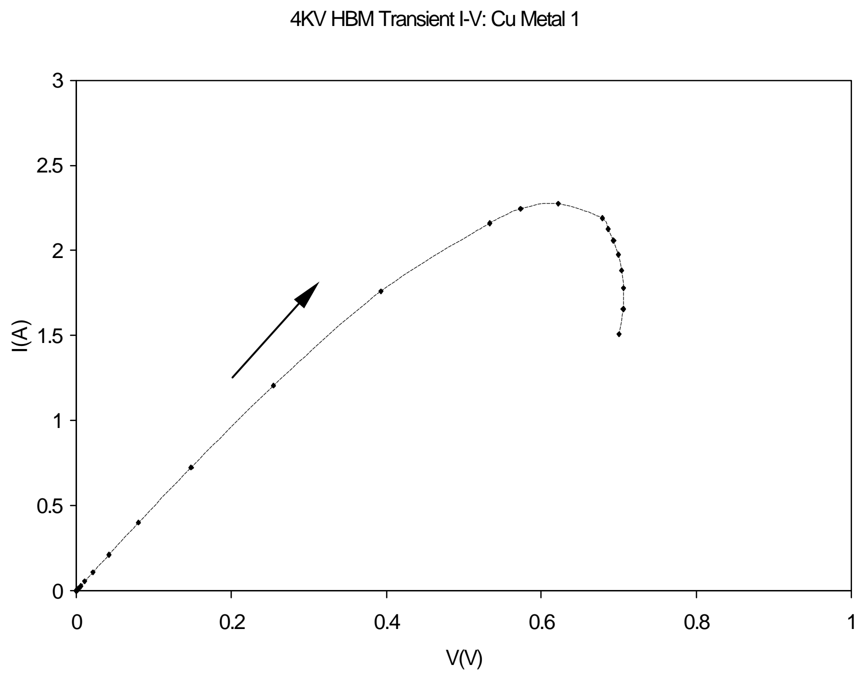
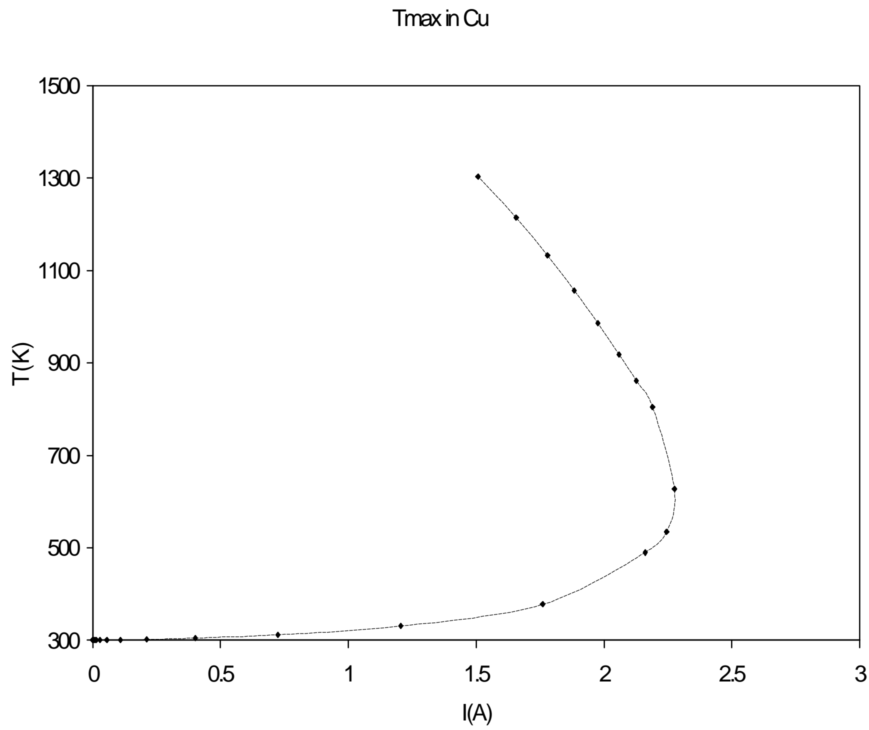


(*Fig. 11a)*
I-V characteristics of a single Cu metal line under 4KV transient ESD pulse.



(*Fig. 11b)*
T_{max} ~ I curve during a HBM 4KV transient ESD pulse.

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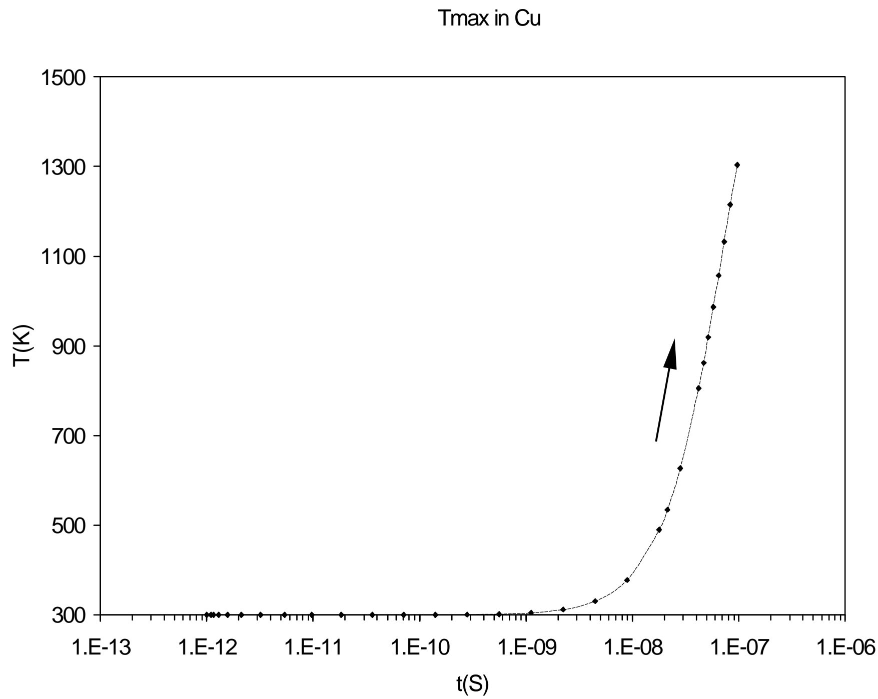

(*Fig. 11c)*

Transient T_{max} variation in the Cu metal line during a 4KV transient ESD pulse.

Fig. 11 ESD characteristics of a single Cu metal line that failed 4KV ESD test with a width of 9μm.

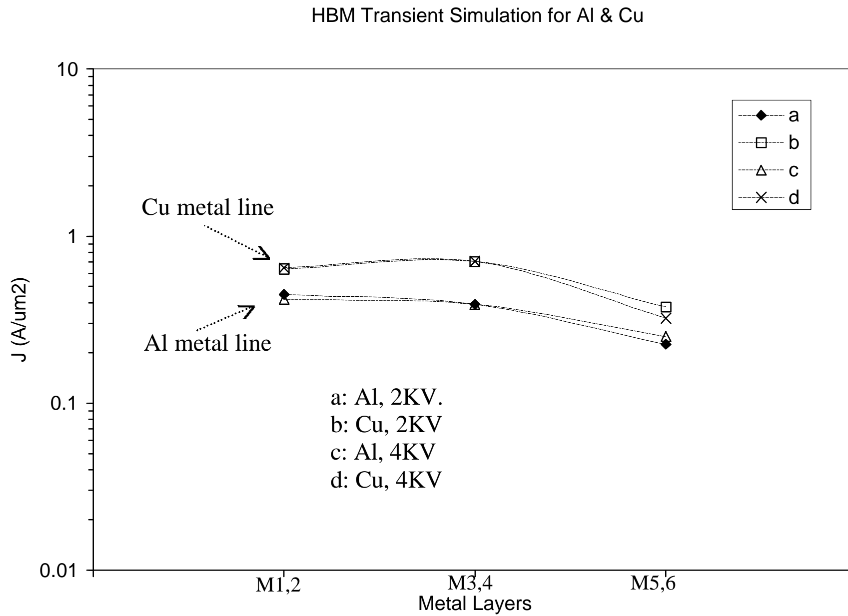

Fig. 12 *a)*

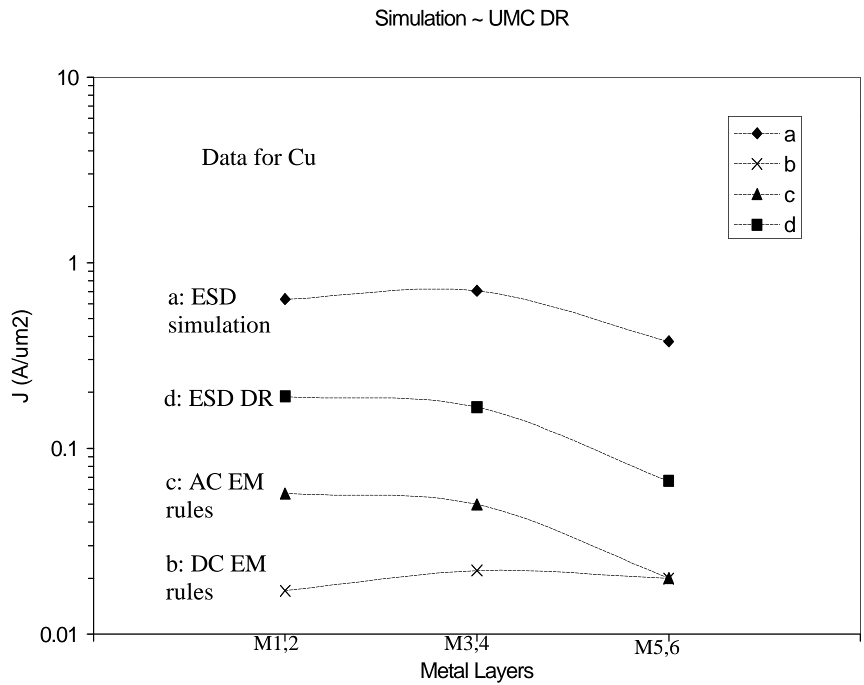

Fig. 12 *b)*

Fig. 12 The maximum sustainable current density *vs.* metal layer characteristics shows good matches between: a) metal layers for both Cu and Al at 2KV and 4KV ESD stressing; and b) ESD simulation results *versus* UMC DR data for Cu.

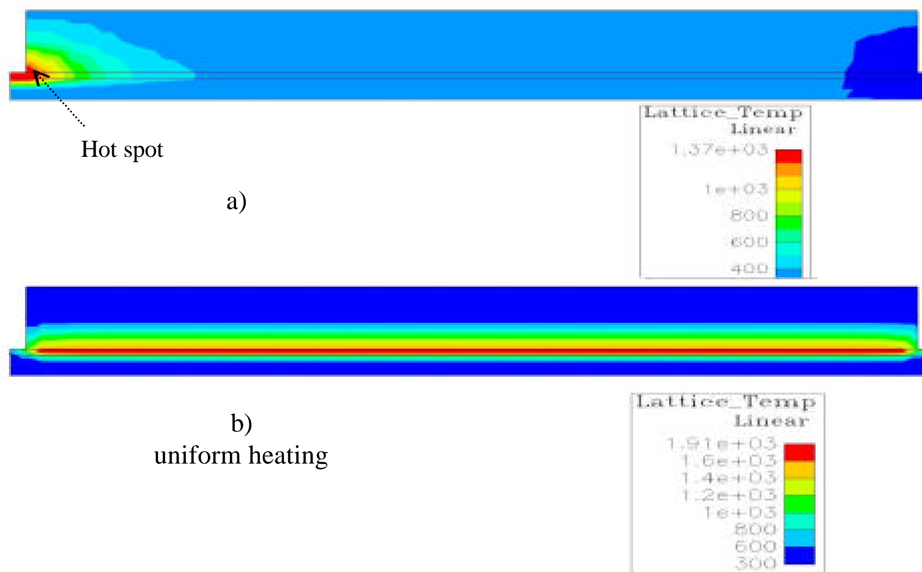

Fig. 13 Metal line temperature distribution maps under ESD stressing: a) localized thermal damage; b) uniform heat distribution.

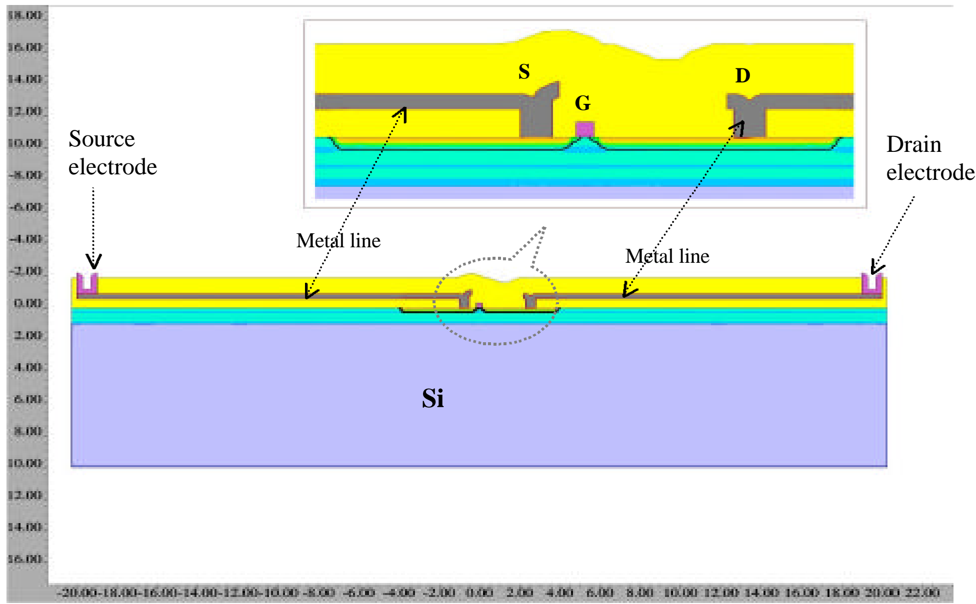

Fig. 14 A cross-section of a complete GGNMOS ESD structure, including metal lines, used in the ESD simulation. Metal 1 layer was used. SCGS, DCGS, 20µm metal line length and dielectric layers were chosen according to UMC ESD design rules.

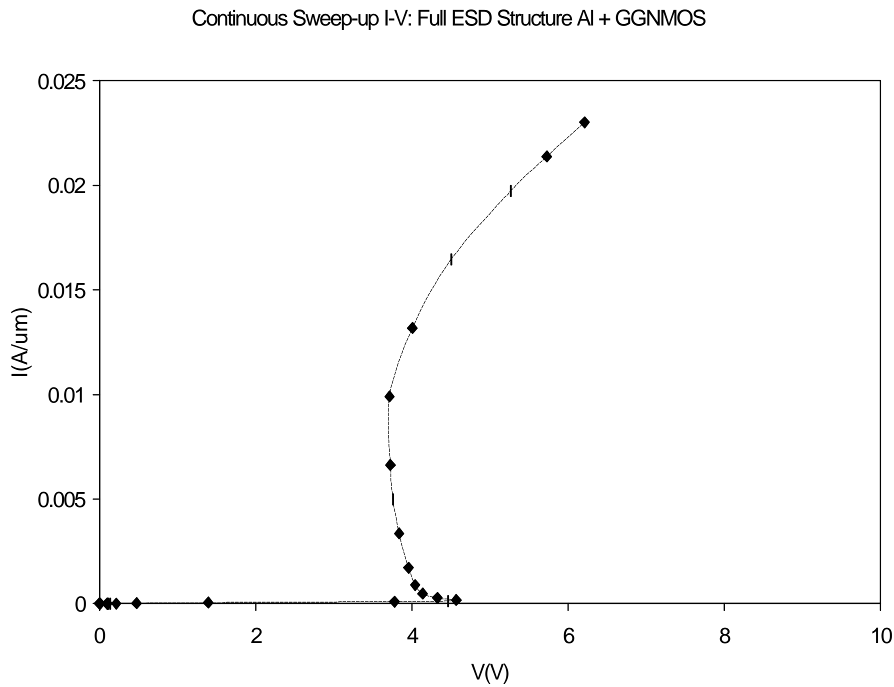

Fig. 15 I-V curve of static ESD simulation for a sample Al ESD device under static ESD stressing.

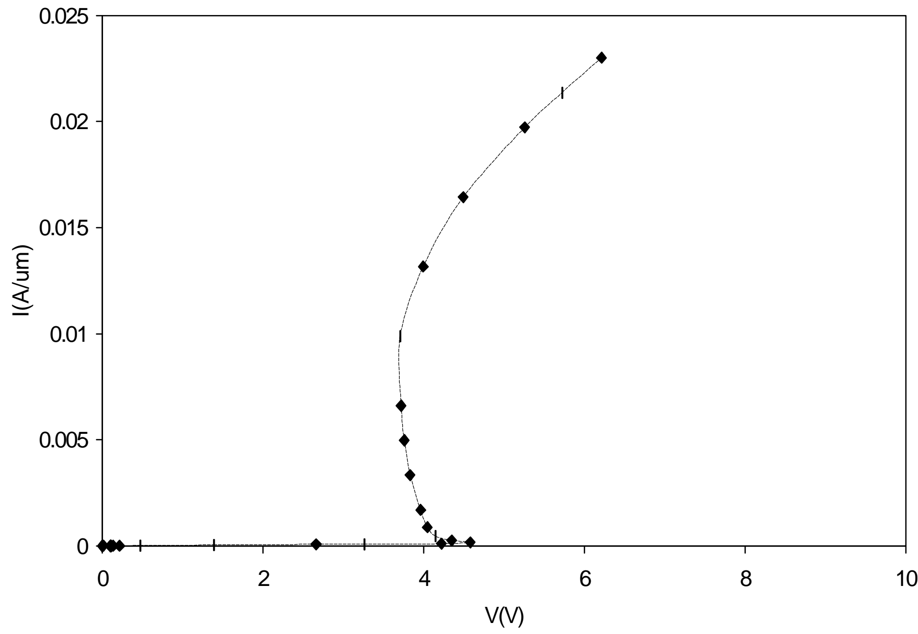

Fig. 16 I-V curve of ESD simulation for a sample Cu ESD device under static ESD stressing.

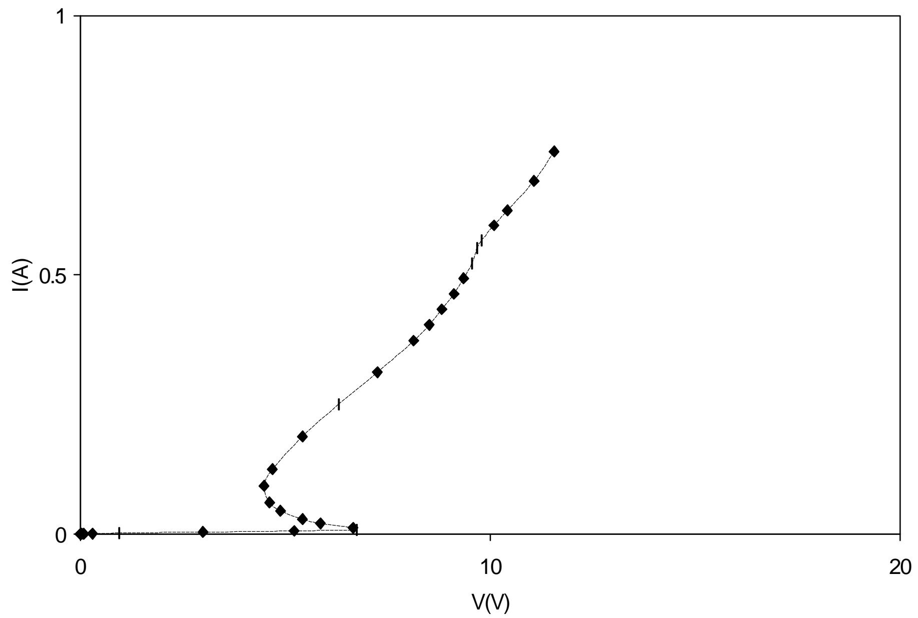

Fig. 17 I-V characteristics of a sample Al ESD device under HBM transient ESD simulation.

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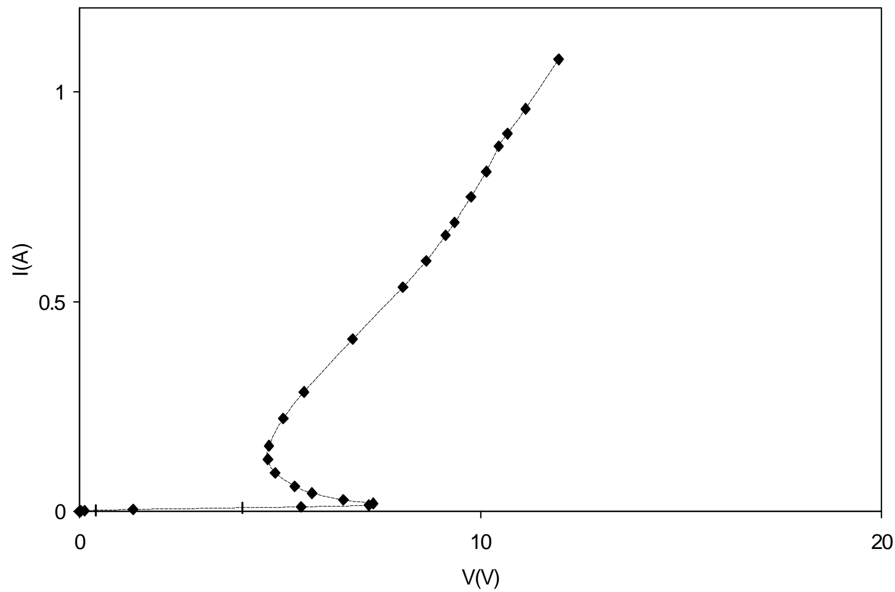

Fig. 18 I-V characteristics of a sample Cu ESD device under HBM transient ESD simulation.

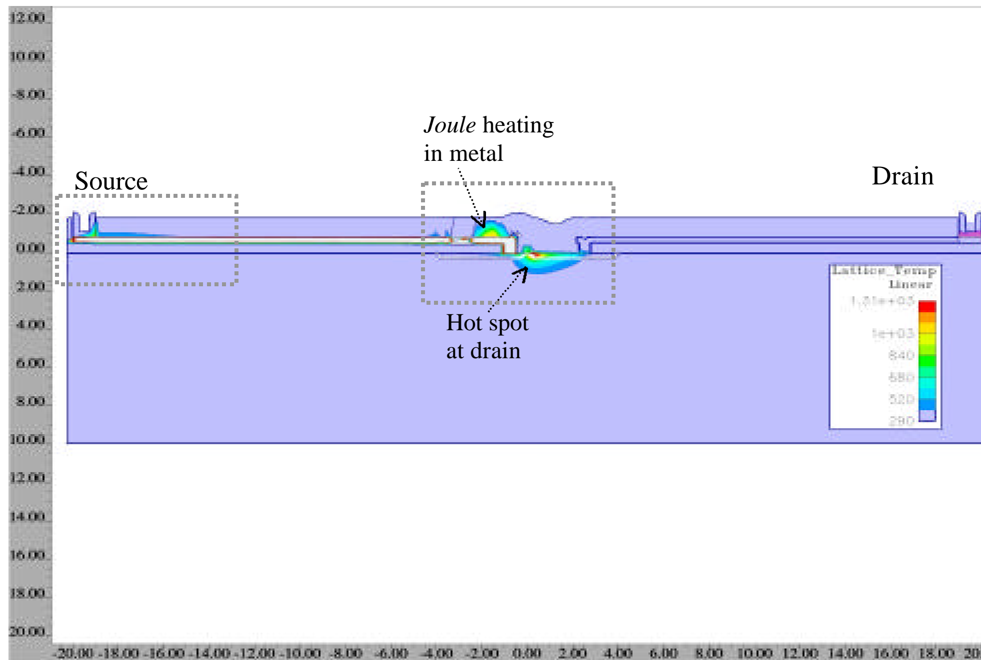

Fig. 19a T_{max} map shows thermal defects in metal lines due to *Joule* heat and in Si channel at the drain junction due to Avalanche.

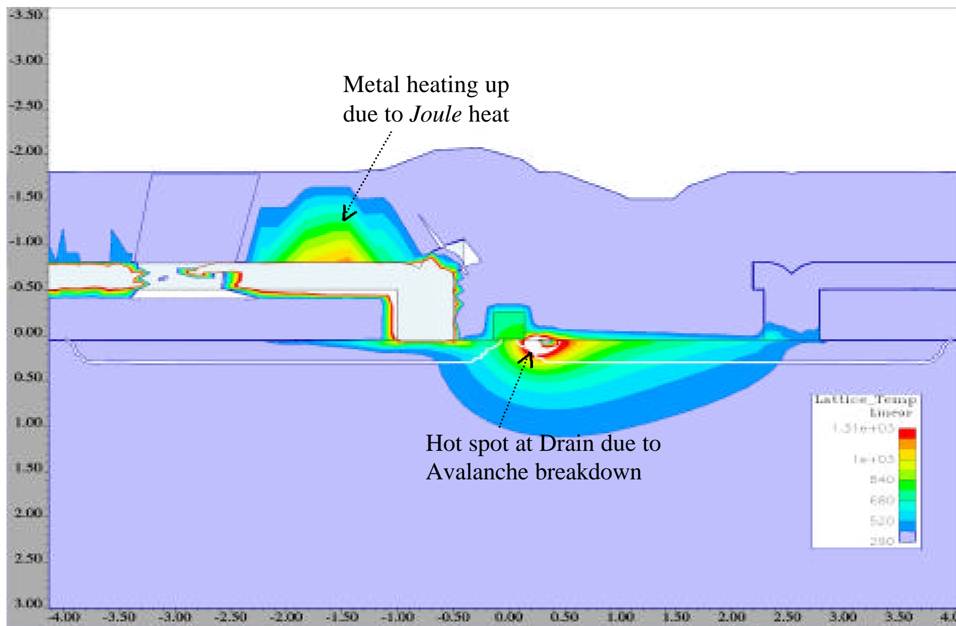

Fig. 19b Enlarged image shows thermal defect in the metal layer as well as in the Si channel.

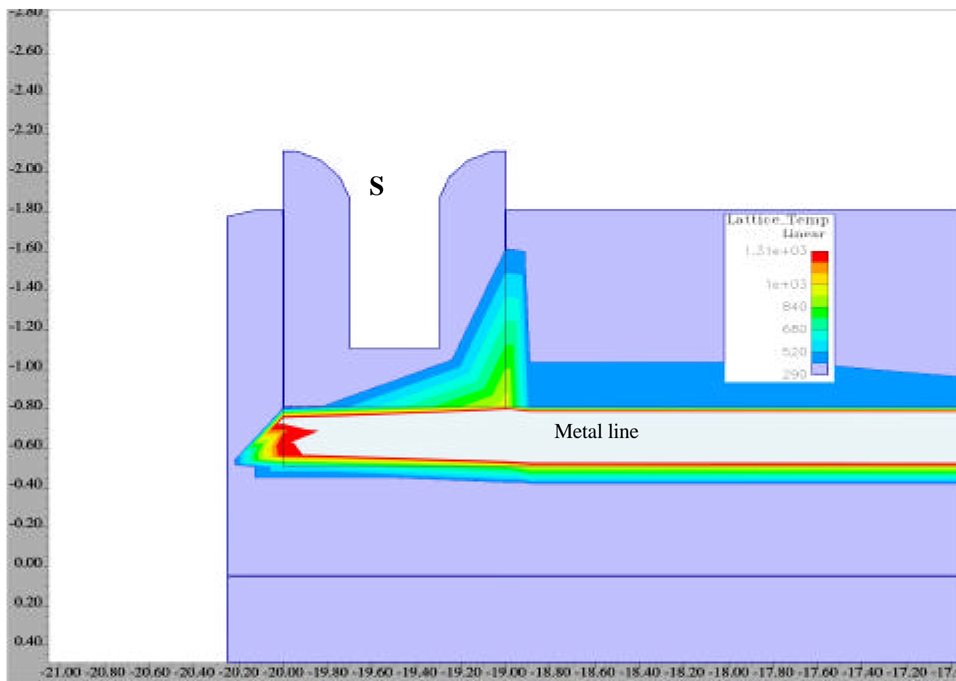

Fig. 19c Enlarged image shows *Joule* heating in metal.

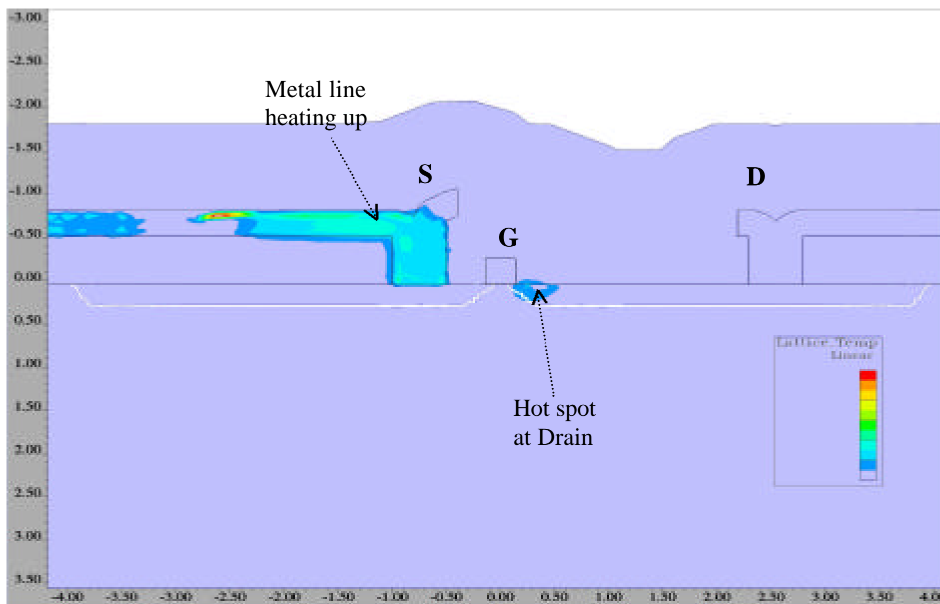

Fig. 19d a better illustration of the T_{max} map using different scale shows heat accumulation inside metal.

Fig. 19 T_{max} contour maps of a sample Cu ESD device under HBM transient ESD simulation shows how *Joule* heating inside the metal lines may lead to thermal damage of the metal lines.

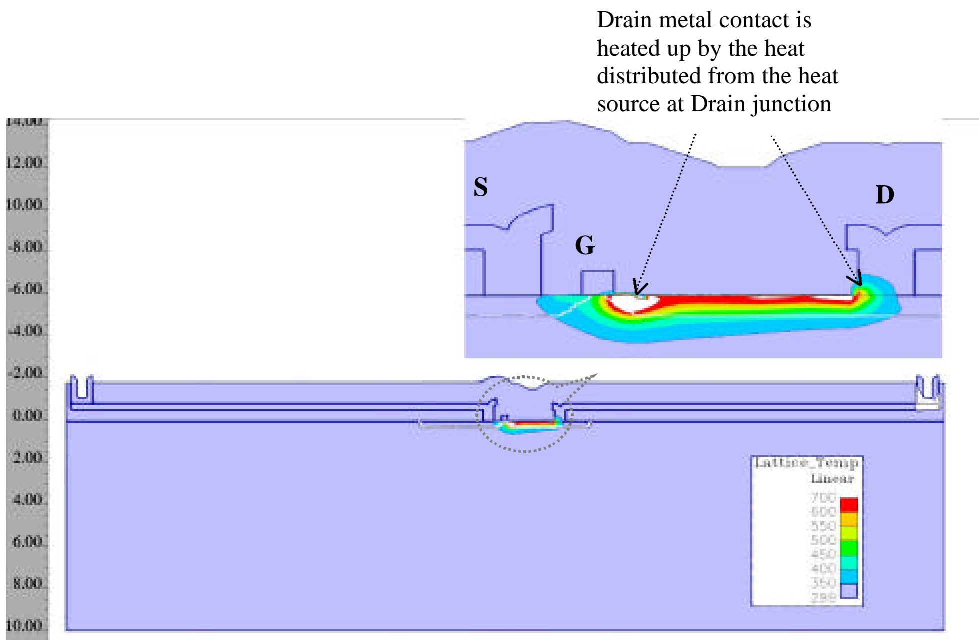

Fig. 20 T_{max} contour map of a sample Cu ESD device shows how the distributing heat from the heat source at the Drain junction in Si channel may heat up the metal contact at the drain end.

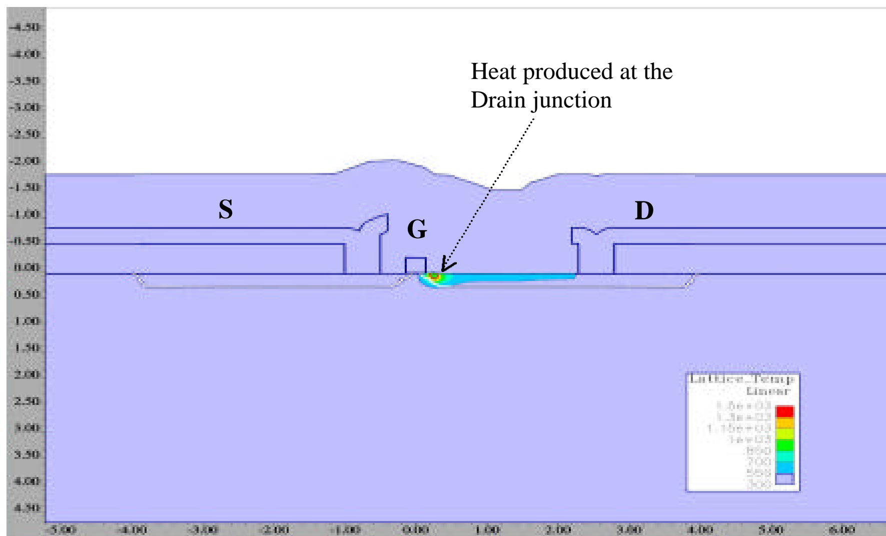

Fig. 21a

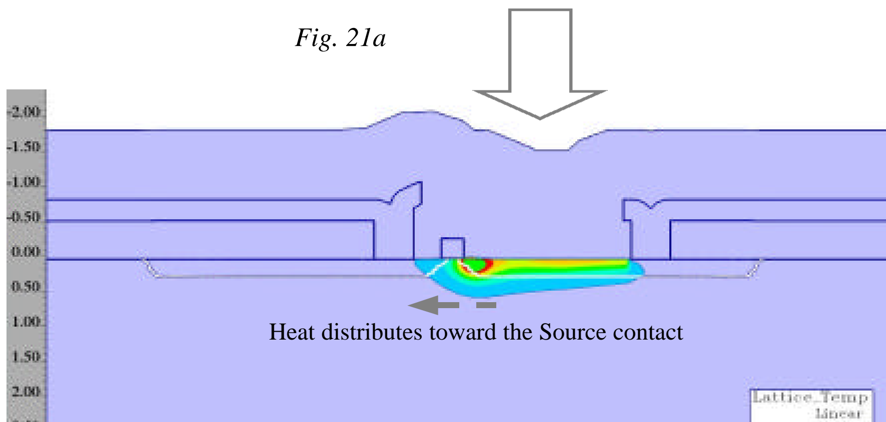

Fig. 21b

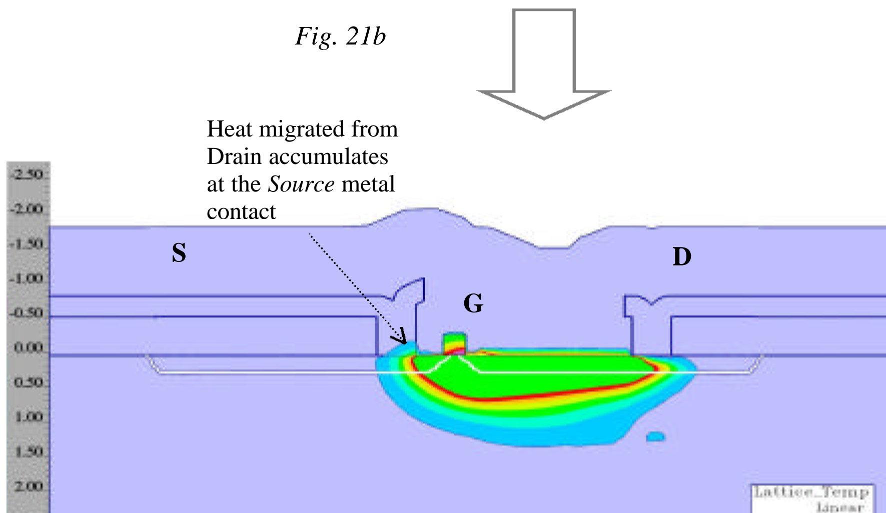

Fig. 21c

Fig. 21 T_{max} contour map of a sample Cu ESD device shows how the distributing heat from the heat source at the Drain junction in Si channel may heat up the metal contact at the Source end also. It indicates that minimum SCGS dimension can not be used in VDSM ESD designs.

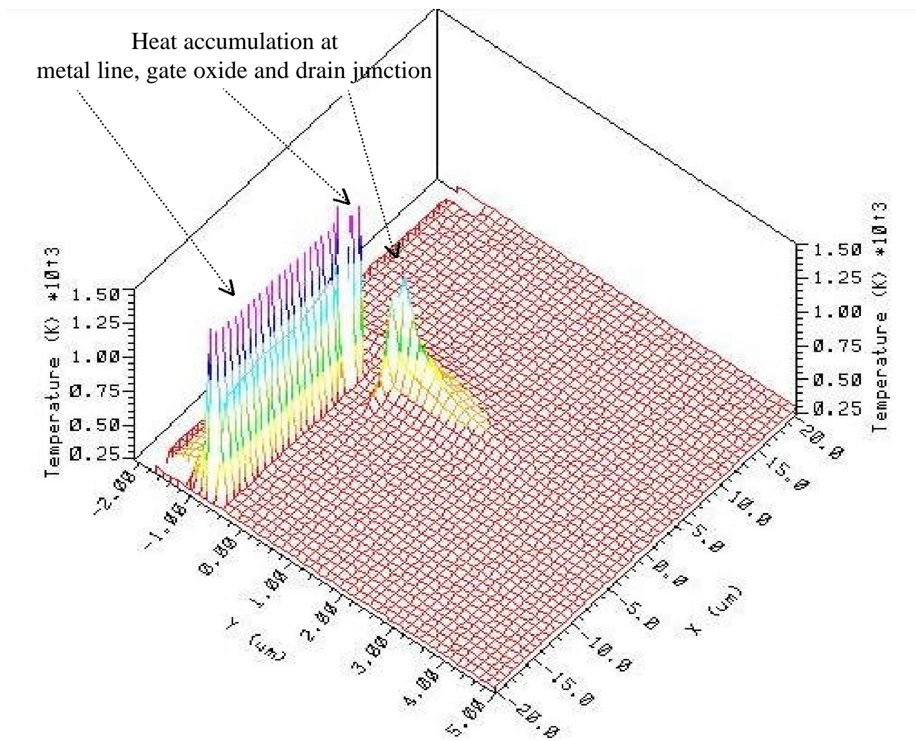

Fig. 22 A 3D T_{max} contour map of a sample Cu ESD device under transient ESD simulation shows heating spots in metal lines, gate oxide, and at drain junction.

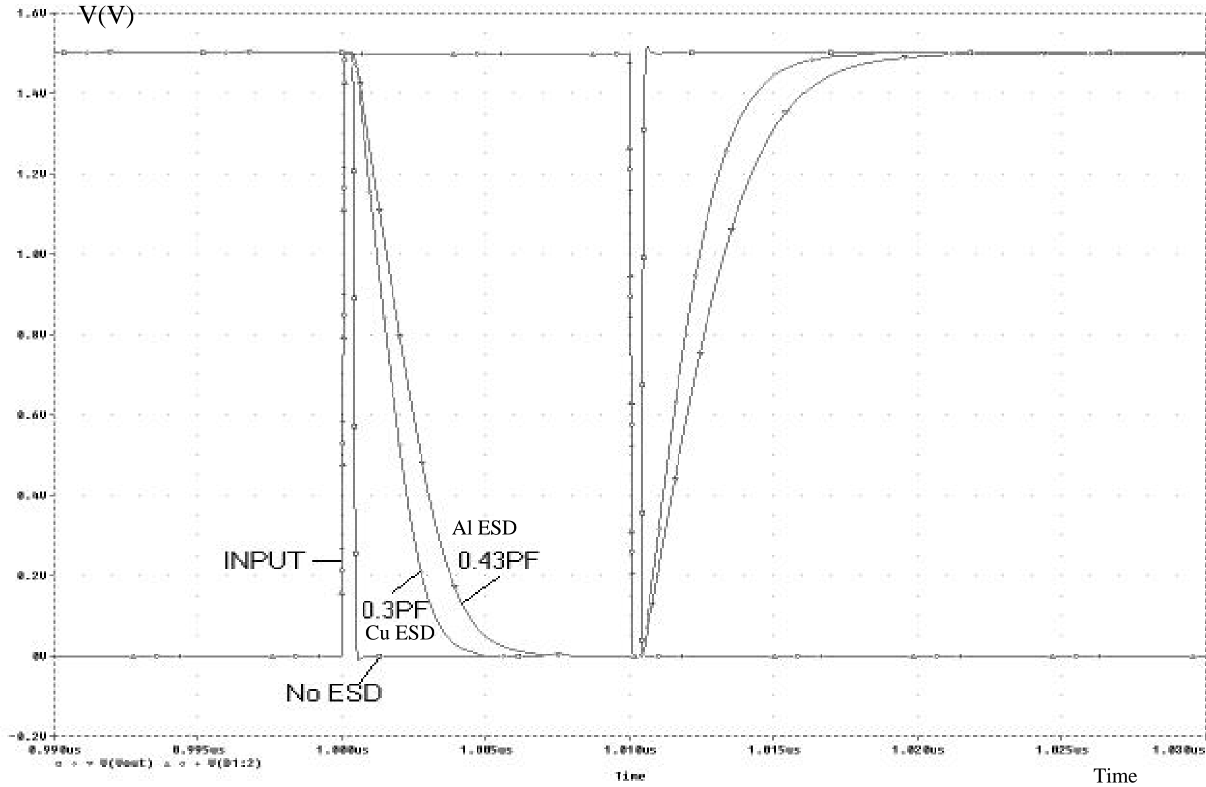

Fig. 23 Input-output wave-forms of a 15-stage ring oscillator circuit with single ESD load.

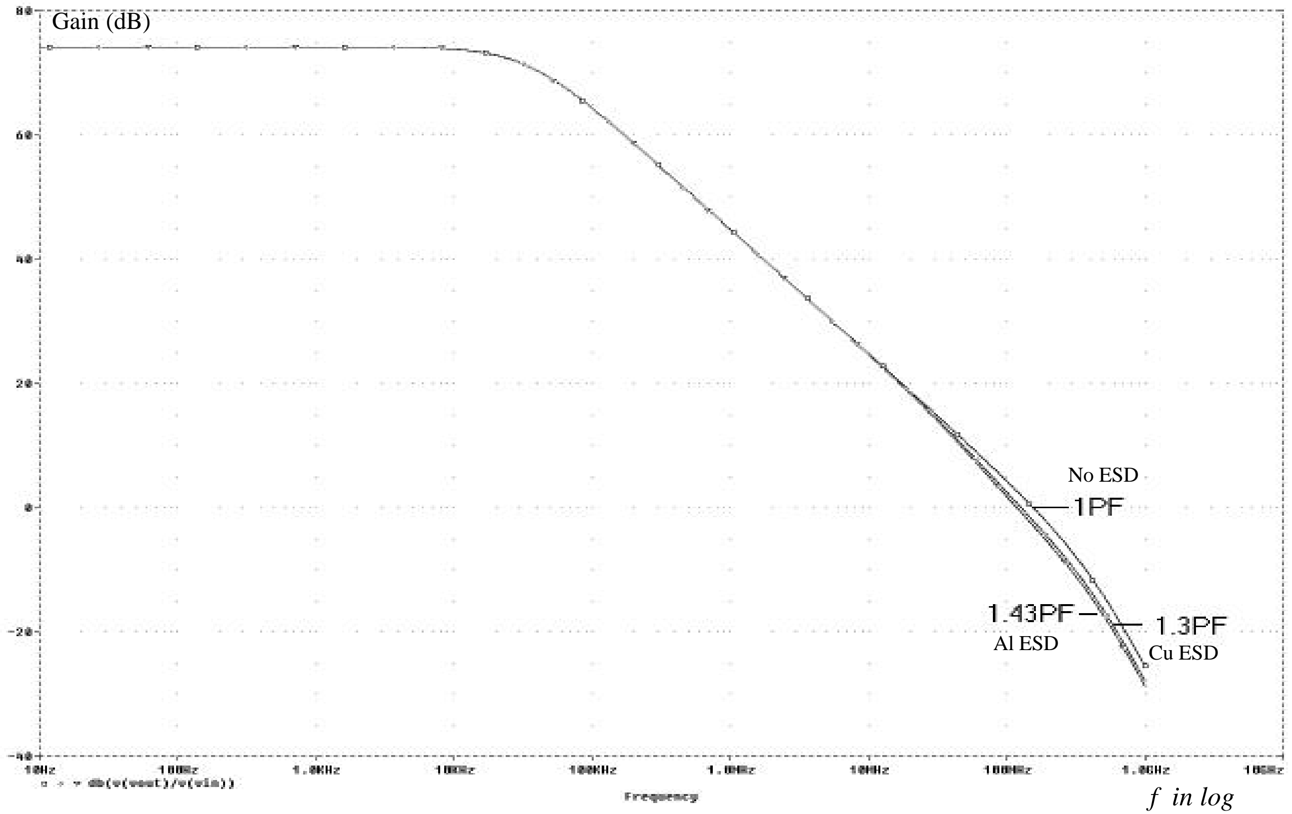

Fig. 24 A gain plot of the Op Amp circuit with C_{ESD} load.

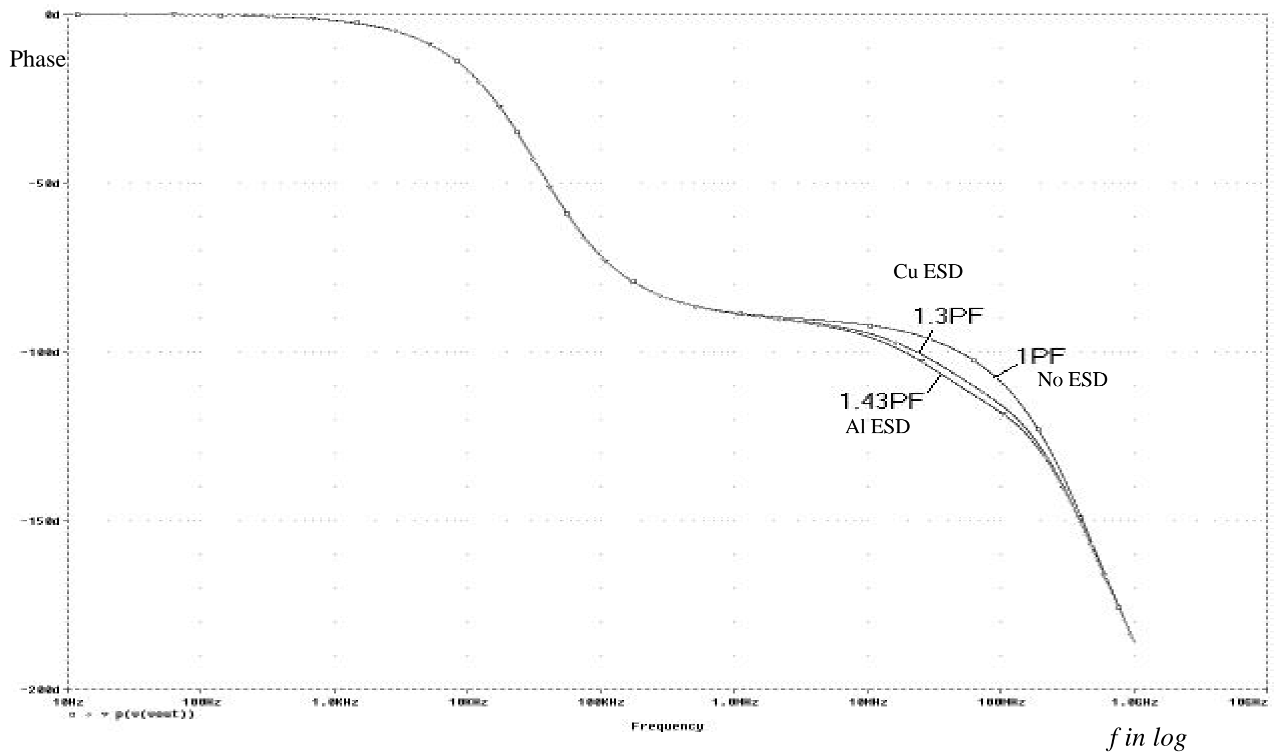

Fig. 25 A Phase plot of the Op Amp circuit with C_{ESD} load.

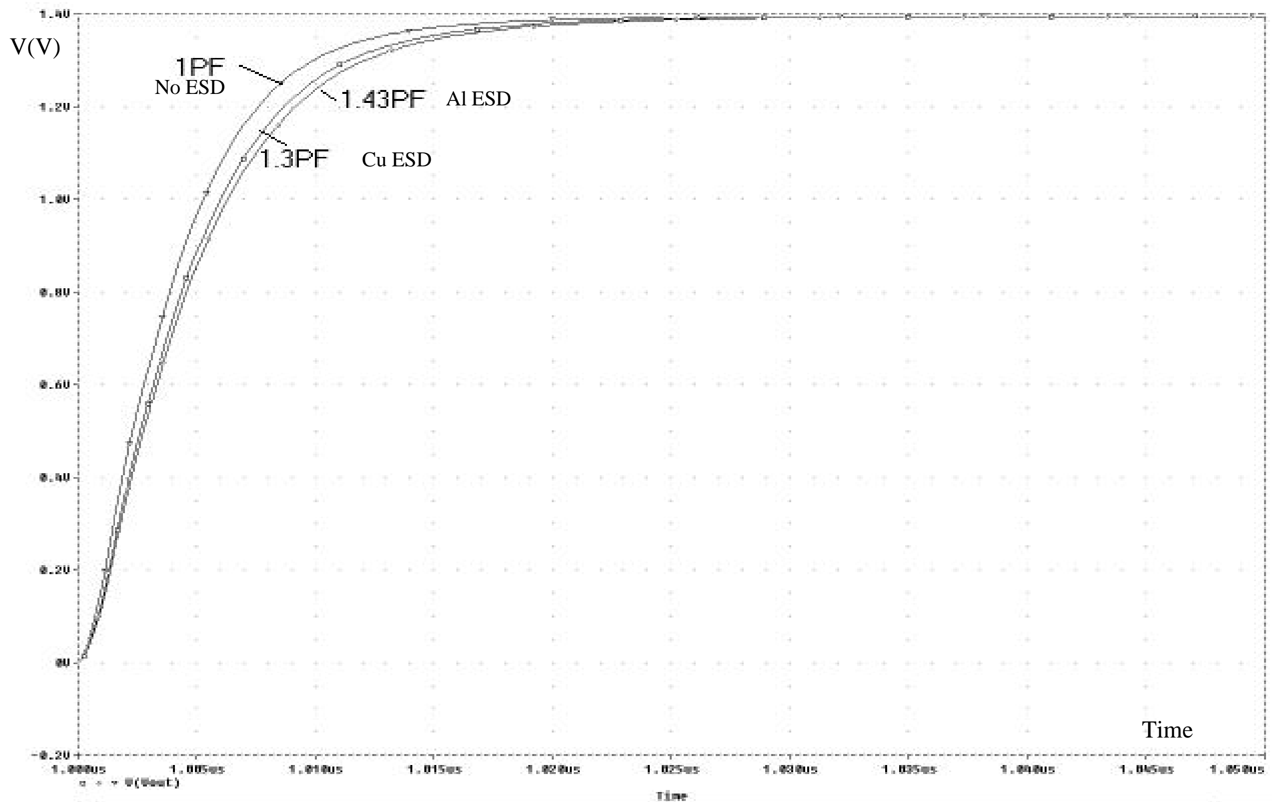

Fig. 26 A large-signal step response plot of the Op Amp circuit with C_{ESD} load for slew-rate test.

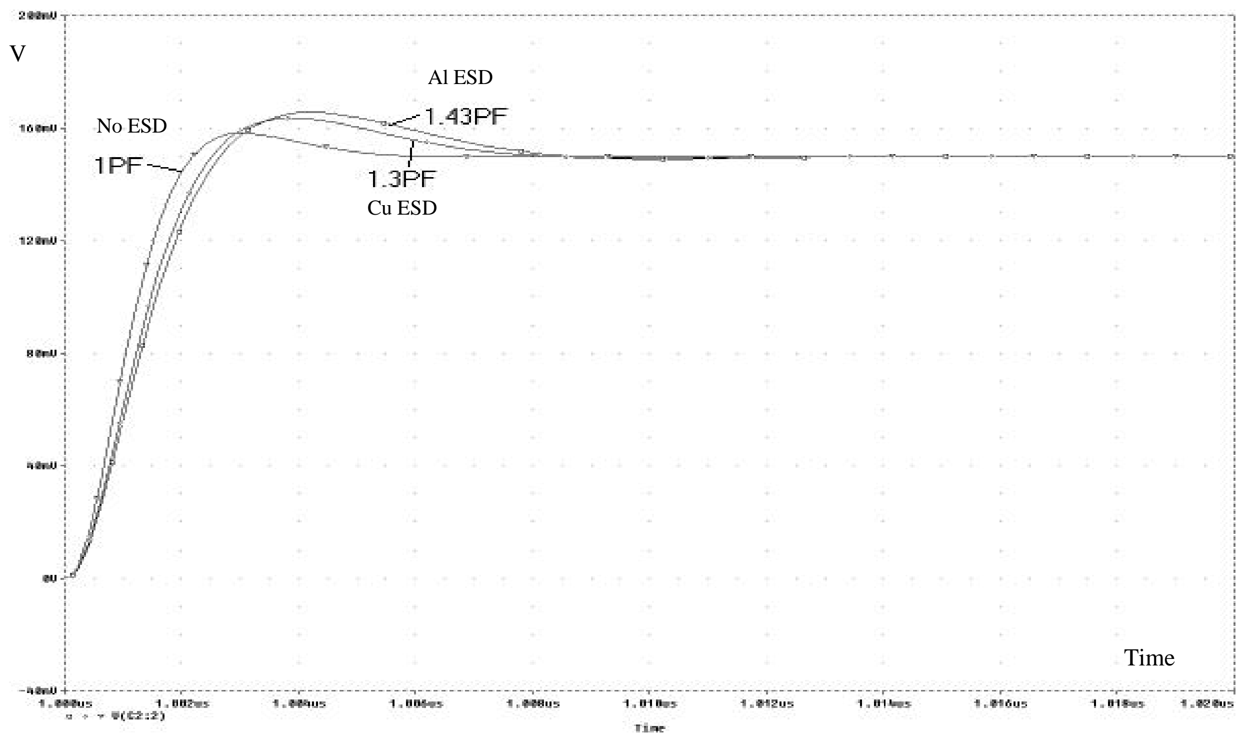

Fig. 27 A small-signal step response plot of the Op Amp circuit with C_{ESD} load for settling-time test.

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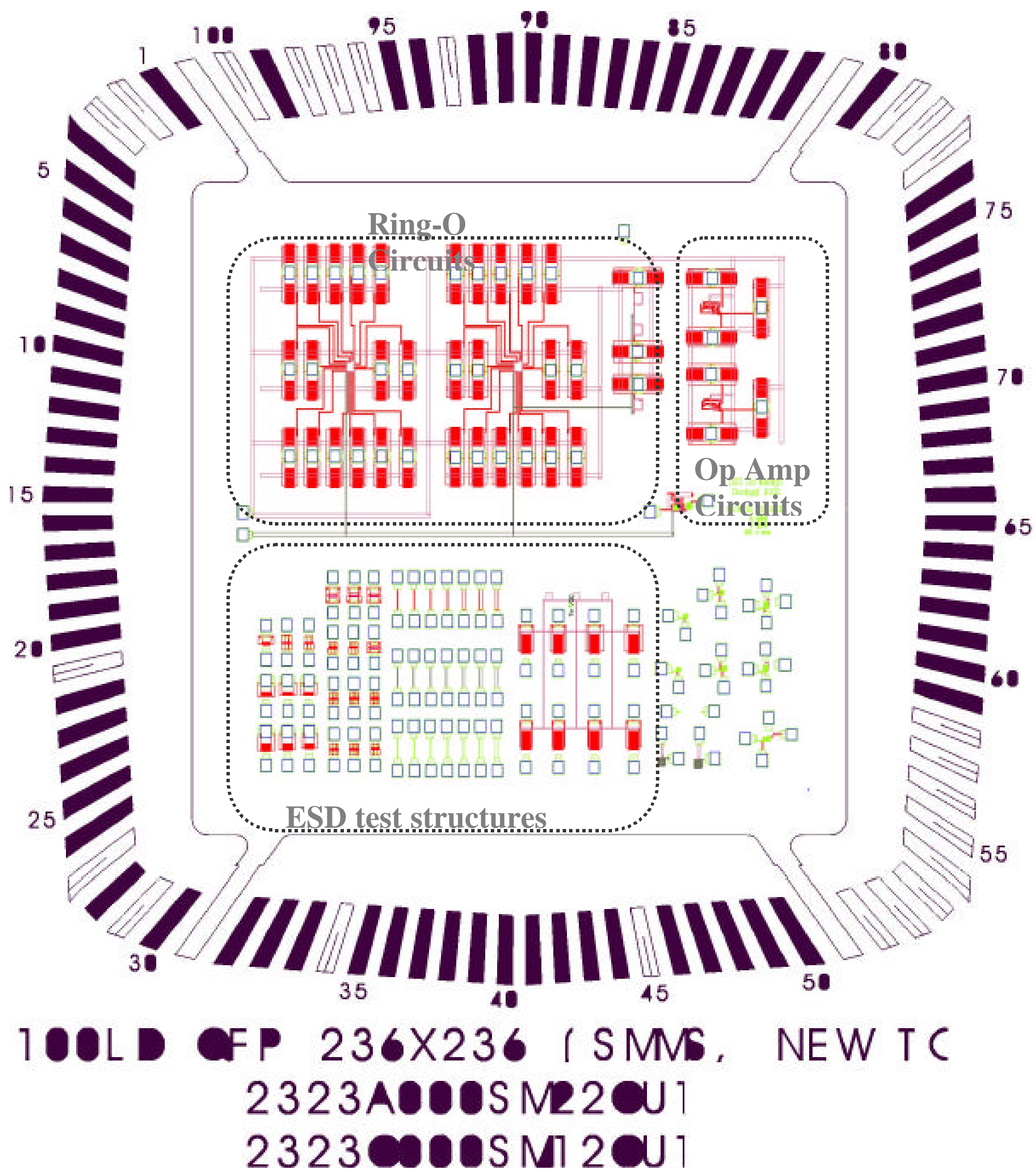

Fig. 28 Layout floor plan: The upper portion consists of the oscillator and Op Amp circuits. The lower portion comprises individual ESD test devices.

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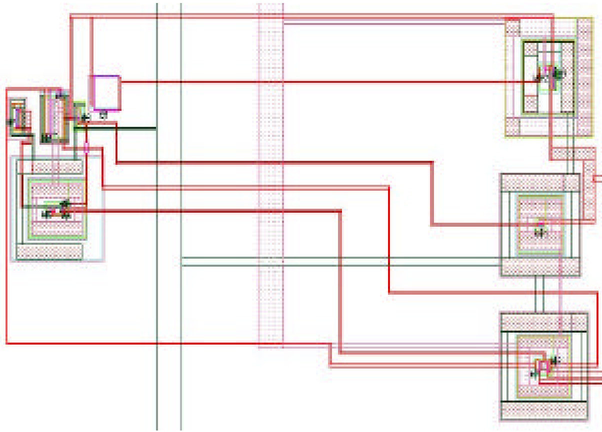
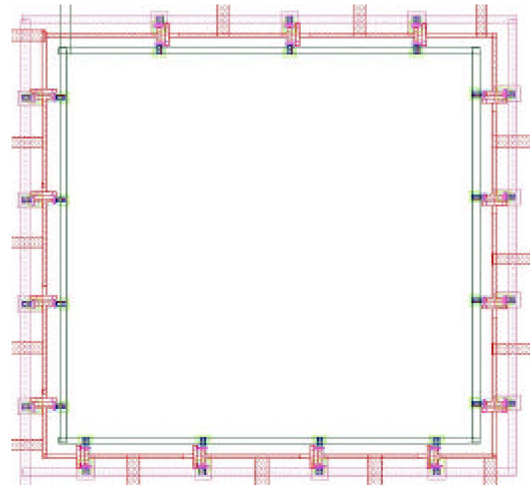
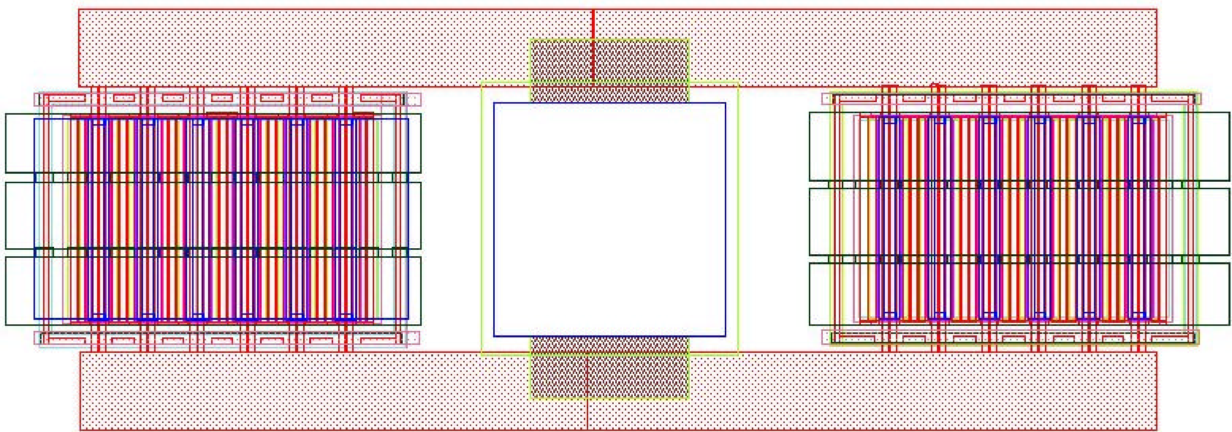


(a) Op Amp Circuit.



(b) Ring oscillator circuit



(c) Pad with complete GGMOS ESD protection to Vdd and Vss.

Fig. 29 Layout views for the circuit portion of the chip.

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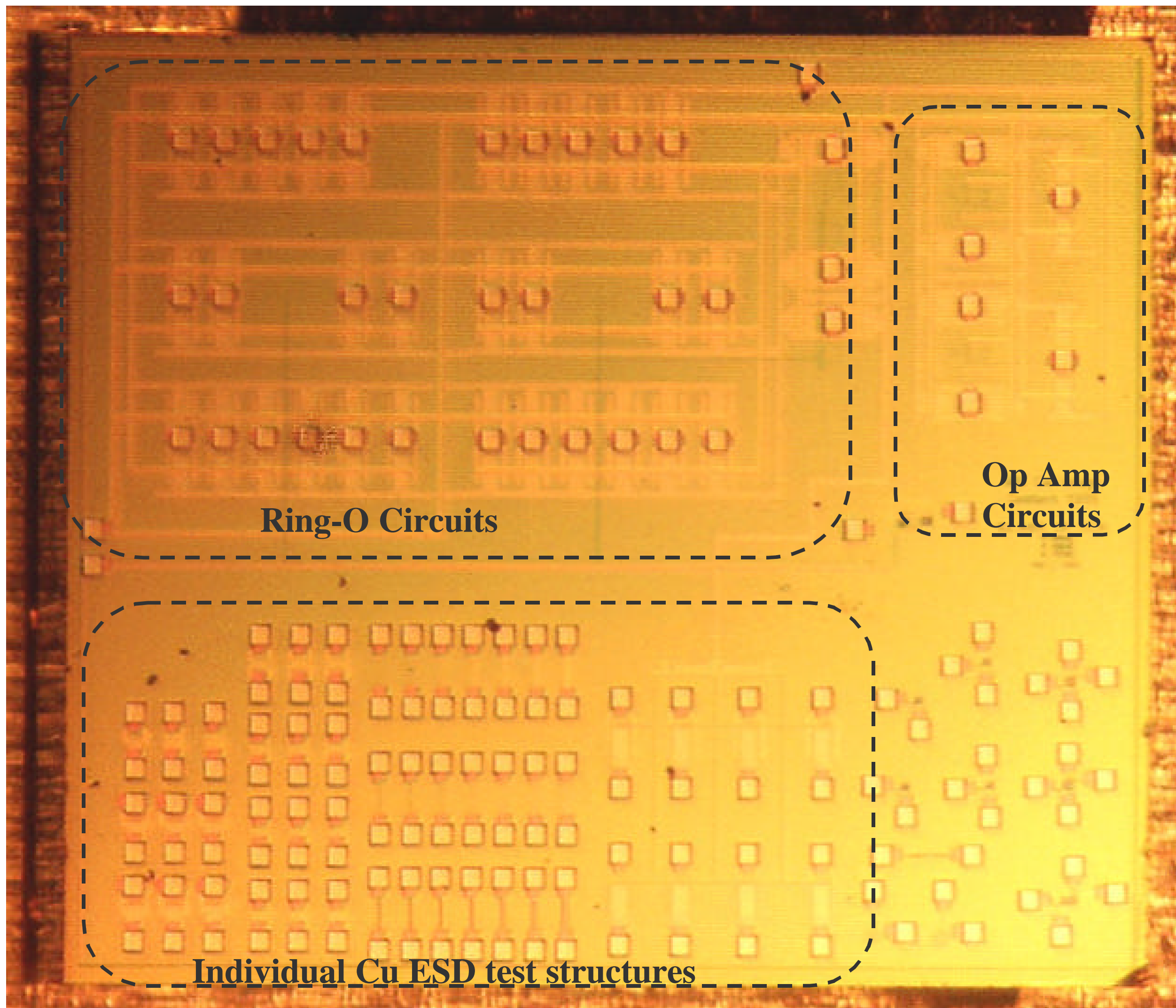

Fig. 30 Die photo of the chip.

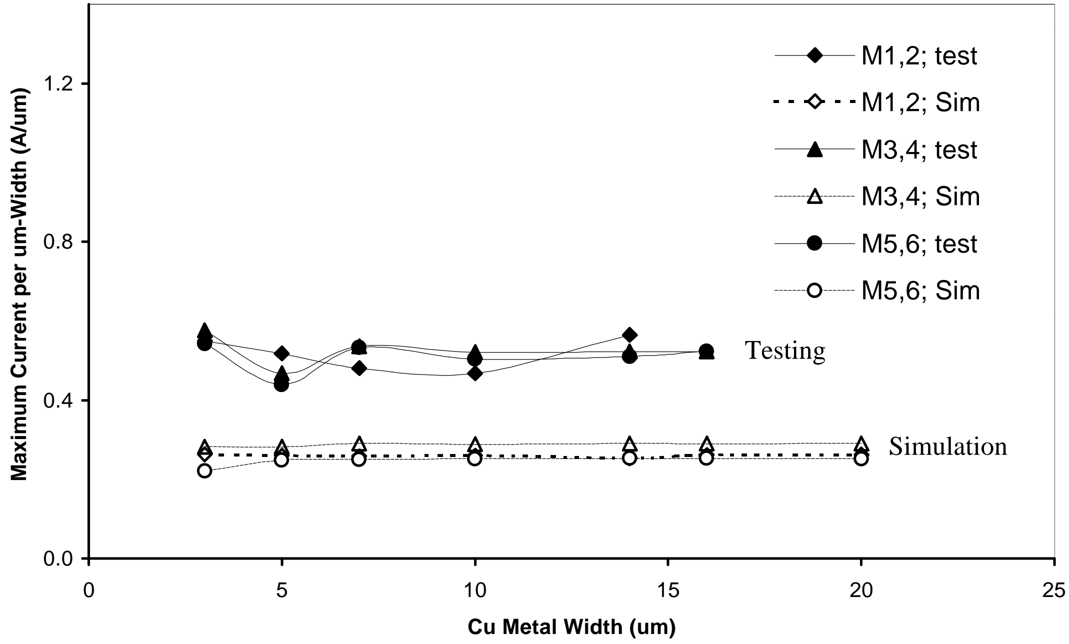

Fig. 31 Maximum sustainable current per width versus metal line-width from simulation and measurements match each other within a constant factor of 2.

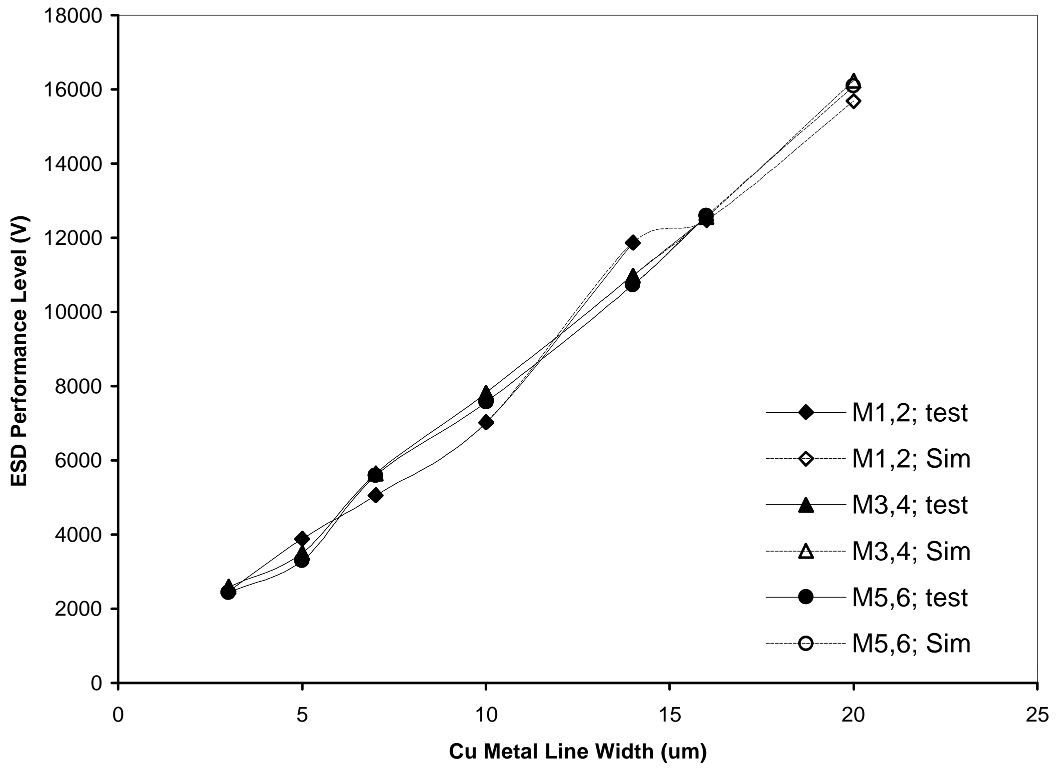

Fig. 32 ESDV level versus Cu metal line-width from simulation and measurements.

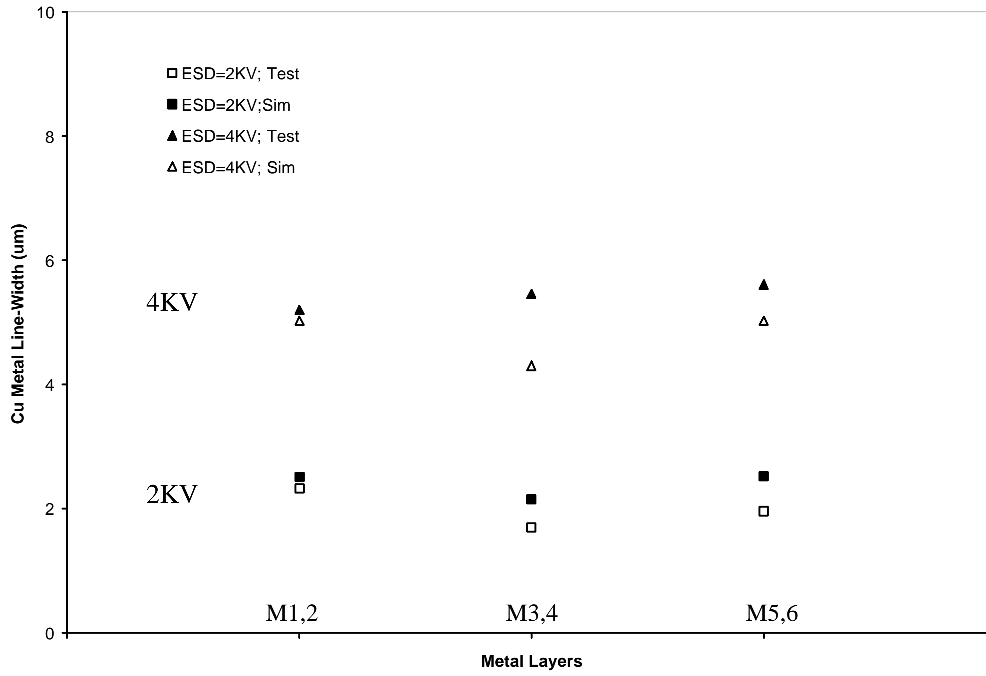

Fig. 33 Cu metal line-width needed for all six layers for ESD=2KV & 4KV from simulation and measurements show good match.

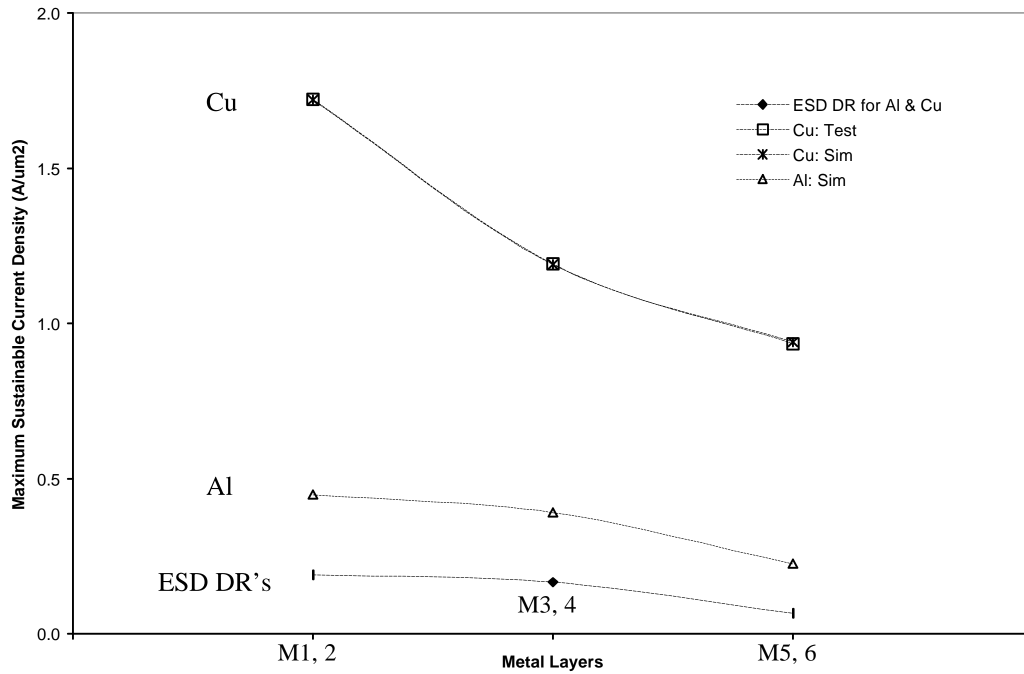

Fig. 34 Maximum sustainable current density (ESD protection level) versus mater layers for Cu, Al and ESD design rules from simulation and measurements show that Cu posses superior ESD performance property to Al.